



**E X C E L L E N C E   I N   M A C H I N E   V I S I O N**

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<http://www.imaging.com>

# **X64-CL Series**

## **User's Manual**

**Part number OC-64CM-CLU00**

**Edition 1.22**



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# Introduction

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## Overview of the Manual

The X64-CL Series *User's Manual* covers the following topics:

- **Overview of the X64-CL Series**  
Description of the X64-CL package and a brief summary of its capabilities.
- **Installing the X64-CL**  
Installation procedures for the X64-CL board and driver under Windows NT or Windows 2000 or Windows XP, as well as information on camera connectivity.
- **CamExpert Quick Start for the X64-CL**  
User's guide to interfacing cameras with CamExpert.
- **The Spera Demo Application**  
Using the Spera Acquisition demo programs to test the X64-CL installation.
- **X64-CL Reference**  
Descriptions of X64-CL hardware, block diagram, capabilities, and acquisition modes supported.
- **X64-CL Spera Servers & Resources**  
Specifications specific to the Spera Imaging Library.
- **Technical Specifications**  
Connector locations and pin-out descriptions.
- **CameraLink Interface**  
Overview of the CameraLink specification.
- **Coreco Imaging Contact Information**  
Phone numbers, web site, and important email addresses.

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## About the Manual

This manual exists in printed, compiled HTML help, and Adobe Acrobat (PDF) formats. The help and PDF formats make full use of hypertext cross-references and include links to the Coreco Imaging home page on the Internet, located at <http://www.imaging.com/>, accessed using any web browser.

For information specific to the X64-CL, visit the Coreco Imaging web site at [www.imaging.com](http://www.imaging.com) or <http://www.x64.info/>.

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## Using the Manual

File names, directories, and Internet sites will be in bold text (e.g., **image2.bmp**, **c:\sapera**, **http://www.imaging.com**).

Text that must be entered using the keyboard will be in typewriter-style text (e.g., **c:\temp**).

Menu and dialog actions will be indicated in bold text in the order of the instructions to be executed, with each instruction separated by bullets. For example, going to the **File** menu and choosing **Save** would be written as **File•Save**.

The X64-CL series consists of two product models, X64-CL Dual and X64-CL Full. Unless a model is explicitly mentioned the name X64-CL describes both models.

# Overview of the X64-CL Series

## X64-CL Package

### X64-CL Board Family

Item	Product Number
<b>66MHz Pixel Clock</b> X64-CL Full with 32 MB of memory X64-CL Full with 128 MB of memory	OC-64C0-00080 <sup>1</sup> OC-64C0-02080 <sup>1</sup>
<b>85MHz Pixel Clock</b> X64-CL Full with 32 MB of memory X64-CL Full with 128 MB of memory X64-CL Full with 256 MB of memory X64-CL Full with 1 GB of memory X64-CL Full with 2 GB of memory	OC-64C0-10080 <sup>1</sup> OC-64C0-12080 <sup>1</sup> OC-64C0-13080 <sup>2</sup> OC-64C0-15080 <sup>2</sup> OC-64C0-16080 <sup>2</sup>
<b>66MHz Pixel Clock</b> X64-CL Dual with 32 MB of memory X64-CL Dual with 128 MB of memory X64-CL Dual with 256 MB of memory	OC-64C0-00060 <sup>1</sup> OC-64C0-02060 <sup>1</sup>
<b>85MHz Pixel Clock</b> X64-CL Dual with 32 MB of memory X64-CL Dual with 128 MB of memory X64-CL Dual with 256 MB of memory X64-CL Dual with 1 GB of memory X64-CL Dual with 2 GB of memory	OC-64C0-10060 <sup>1</sup> OC-64C0-12060 <sup>1</sup> OC-64C0-13060 <sup>2</sup> OC-64C0-15060 <sup>2</sup> OC-64C0-16060 <sup>2</sup>
Optional Hirose Connector Module (CMI #194) see "X64-CL Connector View" <a href="#">on page 81</a>	Contact Sales at Coreco Imaging
Sapera version 4.20 or later Sapera Imaging Development Library includes: <ol style="list-style-type: none"><li>1. Sapera LT: Provides everything you will need to build your imaging application</li><li>2. Sapera: Over 600 optimized image processing routines</li><li>3. Current Sapera compliant board hardware drivers &amp; documentation</li></ol>	Contact Sales at Coreco Imaging
Note 1: see "X64-CL Layout Drawings" <a href="#">on page 77</a> for board layout Note 2: see "X64-CL EM Revision A2 Layout Drawing" <a href="#">on page 79</a> for board layout	

## X64-CL Cables & Accessories

Item	Product Number
I/O Interface Connector Bracket Assembly supplied with each X64-CL (connects to J4)	OC-64CC-0TIO1
Power interface cable required when supplying power to cameras	OC-COMC-PCPWR
CameraLink Video Input Cable (optional product): 1 meter 2 meter	OC-COMC-CLNK0 OC-COMC-CLNK6
DB25 male to color coded blunt end cable – 6 foot (1.82 meter) length	OC-COMC-XEND1

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# About the X64 Series of Frame Grabbers

## X64-CL Series Key Features

- Two Models available:
  - **X64-CL Full:** 1 Full or 1 Medium or 1 Base Camera
  - **X64-CL Dual:** 1 or 2 Base Cameras
    - Simultaneous capture from 2 Base cameras
    - Cameras do not need to be synchronized
    - Can mix monochrome and color cameras
- Targeted for general purpose machine vision applications
- Two CameraLink interface (MDR26) connectors
- Single slot
- 32MB-2GB frame buffer memory
- Trigger input (TTL or LVDS software selectable)
- Quadrature Shaft encoder input
- Camera control signals
- Dual Strobe Outputs

## User Installed Specialized Firmware

Certain non-standard cameras required specific X64-CL firmware designed to support the enhanced specifications of those cameras. Using the X64-CL firmware loader utility, standard or specialized firmware is easily installed, either during driver installation or later when the imaging application changes. Firmware versions currently available are:

- **X64-CL Standard (default)**  
Support for up to 8-Tap cameras with 8-bit or 10-bit LUT (see "Firmware: Standard (default)" [on page 61](#) for details on these LUT modes). See "X64-CL Spera Capabilities" [on page 66](#) for a complete listing of capabilities.
- **X64-CL 12-Bit LUT**  
Support for 12-Bit LUT with 12-Bit monochrome or 3x12-Bit RGB sources. This firmware offers the same functionality as the "Standard" one, except for the LUT support. See "Firmware: X64-CL-DUAL 12-bit LUT" [on page 62](#) for details on these LUT modes.
- **X64-CL 10-Tap Format 1** (not a CameraLink standard),  
Firmware for the X64-CL 85 MHz to support cameras such as the Vosskuhler CMC-1300. See "Firmware: X64-CL 10-Tap Format 1" [on page 63](#) for addition details.
- **X64-CL 10-Tap Format 2** (not a CameraLink standard),  
Firmware for the X64-CL 85 MHz to support cameras such as the Basler A504K. See "Firmware: X64-CL 10-Tap Format 2" [on page 64](#) for addition details.

# ACUPlus: X64-CL Acquisition Control Unit

ACUPlus consists of two sets of independent grab controllers, one pixel packer, and one time base generator. ACUPlus delivers a flexible acquisition front end plus it supports pixel clock rates of up to 66MHz (85MHz optional).

ACUPlus acquires variable frame sizes up to 256KB per horizontal line and up to 16 million lines per frame. ACUPlus can also capture an infinite number of lines from a linescan camera without losing a single line of data.

ACUPlus supports standard CameraLink multi-tap configurations from 8 to 24-bit/pixels. Additionally, alternate tap configurations can support up to 8 taps of 8-bits each.

X64-CL Dual supports two cameras with different tap configurations simultaneously such as one dual tap 8/10/12-bits monochrome camera with an RGB 24-bit camera.

## CameraLink Maximum Acquisition Rates:

This table specifies the X64-CL acquisition hardware maximums, not the maximum data transfer rate through the PCI 64 bus to system memory.

Cameras connected	CameraLink standard	Maximum Acquisition rate 66 MHz components	Maximum Acquisition rate 85 MHz components
2	Base	396 Mbytes/sec	510 Mbytes/sec
1	Medium	396 Mbytes/sec	510 Mbytes/sec
1	Full	528 Mbytes/sec	680 Mbytes/sec

## DTE: Intelligent Data Transfer Engine

The X64-CL intelligent Data Transfer Engine ensures fast image data transfers between the board and the host computer with zero CPU usage. The DTE provides a high degree of data integrity during continuous image acquisition in a non-real time operating system like Windows. DTE consists of multiple independent DMA units, Tap Descriptor Tables, and Auto-loading Scatter-Gather tables.

# **Advanced Controls Overview**

## **Visual Indicators**

X64-CL features two unique visual LED indicators to facilitate system installation and setup. These provide visual feedback indicating when the camera is connected properly and sending data.

## **General Purpose I/Os**

X64-CL provides a number of interrupt driven general purpose input and output controls via an advanced I/O daughter board module. The optional opto-coupled inputs withstand tough industrial environments. Contact Coreco Imaging for information.

## **External Event Synchronization**

Two sets of dedicated trigger inputs and strobe signals are provided to synchronize precisely image captures with external events.

## **CameraLink Communications ports**

Two PC independent communication ports provide CameraLink controls for camera configurations. These ports do not require addition PC resources like free interrupts or I/O address space. Accessible via the board device driver, the communication ports preset a seamless interface to Windows-based standard communication applications like HyperTerminal, etc. The communication ports are accessible directly from the CameraLink connectors.

## **Quadrature Shaft Encoder**

Important feature for web scanning applications, the Quadrature-Shaft-Encoder inputs allow synchronized line captures from external web encoders.

## **PCI 64 bit Interface**

The X64-CL is a universal PCI slot board, compliant with the PCI version 2.2 specification for 64 bit devices.

The X64-CL operates in:

- 64 bit – 66/33 MHz PCI slots
- 32 bit – 33 MHz PCI slots

Transfer rates up to 528 Mbytes/sec with the appropriate camera are possible. The X64-CL board occupies one computer expansion slot and one chassis opening.

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# Development Software Overview

## Sapera LT Library

Sapera LT is a powerful development library for image acquisition and control. Sapera LT provides a single API across all current and future Coreco Imaging hardware. Sapera LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards.

Sapera LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

## Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

# Installing the X64-CL

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## Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation.

If you do not feel comfortable performing the installation, please consult a qualified computer technician.

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**Never** remove or install any hardware component with the computer power on.

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## Upgrading Spera or any Coreco Imaging Board Driver

When installing a new version of Spera or a Coreco Imaging acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Upgrade scenarios are described below.

### Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are typically distributed as ZIP files available in the Coreco Imaging web site <http://www.imaging.com/downloads>. Board driver revisions are also available on the next release of the Spera CD-ROM.

Often minor board driver upgrades do not require a new revision of Spera. To confirm that the current Spera version will work with the new board driver:

- Check the new board driver ReadMe.txt file before installing, for information on the minimum Spera version required.
- If the ReadMe.txt file does not specify the Spera version, you can contact Coreco Imaging Technical Support (see “Technical Support” on [page 102](#) ).

To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- From the Windows start menu select **Start•Programs•Coreco Imaging•X64 Device Driver•Modify-Repair-Remove**.
- Click on **Remove**.
- When the driver un-install is complete, reboot the computer.

- Logon the computer as an administrator again.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.
- If the new driver is on a Sapera CD-ROM follow the installation procedure described in “Installing X64-CL Hardware and Driver” on page 11.
- Note that you can not install a Coreco Imaging board driver without Sapera LT installed on the computer.

## Sapera and Board Driver Upgrades

When both Sapera and the Coreco Imaging acquisition board driver are upgraded, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- From the Windows start menu select **Start•Programs•Coreco Imaging•X64 Device Driver•Modify-Repair-Remove**.
- Click on **Remove** to uninstall the board driver.
- From the Windows start menu select **Start•Programs•Coreco Imaging•Sapera LT•Modify-Repair-Remove**.
- Click on **Remove** to uninstall Sapera.
- Reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. See “Sapera LT Library Installation” on page 10 and “Installing X64-CL Hardware and Driver” on page 11 for installation procedures.

---

## Sapera LT Library Installation

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Note: to install Sapera LT and the X64-CL device driver, logon to the workstation as an administrator or with an account that has administrator privileges.

---

The Sapera LT Development Library (or ‘runtime library’ if application development is not being performed) must be installed before the X64-CL device driver.

- Insert the Coreco Imaging Sapera CD-ROM. If **AUTORUN** is enabled on your computer, the Coreco Imaging installation menu is presented.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the Coreco Imaging installation menu and install the required Sapera components.
- The installation program will prompt you to reboot the computer.

Refer to *Sapera LT User’s Manual* for additional details about Sapera LT.

---

# Installing X64-CL Hardware and Driver

## In a Windows NT System

- Turn the computer off and open the computer chassis to allow access to the expansion slot area.
- Install the X64-CL into a free 64 bit PCI expansion slot. If no 64 bit PCI slot is available, use a common 32 bit PCI slot. X64-CL supports the plug and play automatic configuration of the PCI specification.
- Close the computer chassis and turn the computer on. Driver installation requires administrator rights for the current user of the computer.
- Insert the Coreco Imaging Sopera CD-ROM. If **AUTORUN** is enabled on your computer, the Coreco Imaging installation menu is presented. Install the X64-CL driver.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the Coreco Imaging installation menu and install the X64-CL driver.
- The driver installation program prompts you to select a **Full Installation** (needed for application development), or a **Run Time** installation (minimal installation required for target systems). Reboot the computer when prompted.
- Reboot the computer when prompted. During the early stages of the Windows reboot, the X64-CL firmware loader application starts. This is described in detail in the following section. Allow Windows to complete its reboot before proceeding.

## In a Windows 2000 or Windows XP System

- Turn the computer off and open the computer chassis to allow access to the expansion slot area.
- Install the X64-CL into a free 64 bit PCI expansion slot. If no 64 bit PCI slot is available, use a common 32 bit PCI slot. X64-CL supports the plug and play automatic configuration of the PCI specification.
- Close the computer chassis and turn the computer on. Driver installation requires administrator rights for the current user of the computer.
- Windows will find the X64-CL and start its **Found New Hardware Wizard**. Click on the **Cancel** button to close the Wizard Application.
- Insert the Coreco Imaging Sopera CD-ROM. If **AUTORUN** is enabled on your computer, the Coreco Imaging installation menu is presented. Install the X64-CL driver.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the Coreco Imaging installation menu and install the X64-CL driver.
- The driver installation program prompts you to select a **Full Installation** (needed for application development), or a **Run Time** installation (minimal installation required for target systems).
- Reboot the computer when prompted. During the early stages of the Windows reboot, the X64-CL firmware loader application starts. This is described in detail in the following section. Allow Windows to complete its reboot before proceeding.
- Windows will display its **Digital Signature Not Found** message. Click on **Yes** to continue the X64-CL driver installation. Reboot the computer when prompted.

## X64-CL Firmware Loader

After Windows boots, the Firmware Loader program automatically executes. Click **OK** to automatically update the X64-CL firmware with standard functionality as supported by the X64-CL hardware version.

Certain non-standard cameras required specific X64-CL firmware designed to support the enhanced specifications of those cameras. The **Select configuration** drop-down menu lists the non-standard firmware available and supported by the installed X64-CL board.

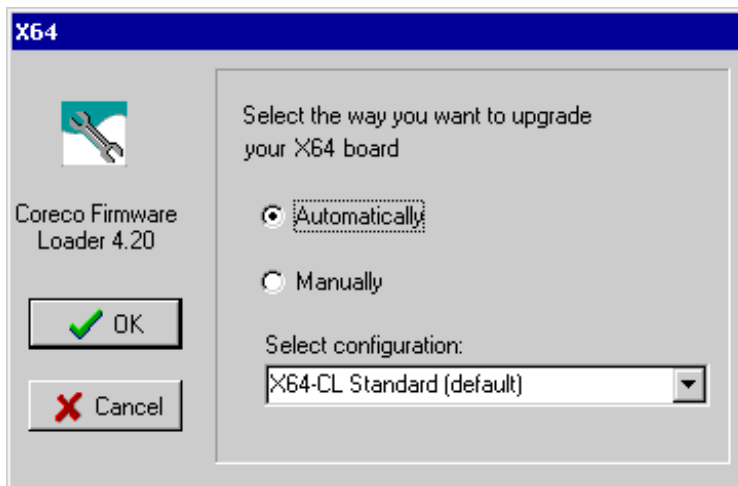
Firmware versions currently available are:

- **X64-CL Standard (default)**  
Support for up to 8-Tap cameras with 8-bit or 10-bit LUT (see "Firmware: Standard (default)" [on page 61](#) for details on these LUT modes). See "X64-CL Samera Capabilities" [on page 66](#) for a complete listing of capabilities.
- **X64-CL 12-Bits LUT**  
Support for 12-Bit LUT with 12-Bit monochrome or 3x12-Bit RGB sources. This firmware offers the same functionality as the "Standard" one, except for the LUT support. See "Firmware: X64-CL-DUAL 12-bit LUT" [on page 62](#) for details on these LUT modes.
- **X64-CL 10-Tap Format 1** (not a CameraLink standard),  
Firmware for the X64-CL 85 MHz to support cameras such as the Vosskuhler CMC-1300. See "Firmware: X64-CL 10-Tap Format 1" [on page 63](#) for addition details.
- **X64-CL 10-Tap Format 2** (not a CameraLink standard),  
Firmware for the X64-CL 85 MHz to support cameras such as the Basler A504K. See "Firmware: X64-CL 10-Tap Format 2" [on page 64](#) for addition details.

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Note: if you are certain that the X64-CL firmware is of the same version as the driver being installed, click on **Cancel** to bypass the update procedure.

---

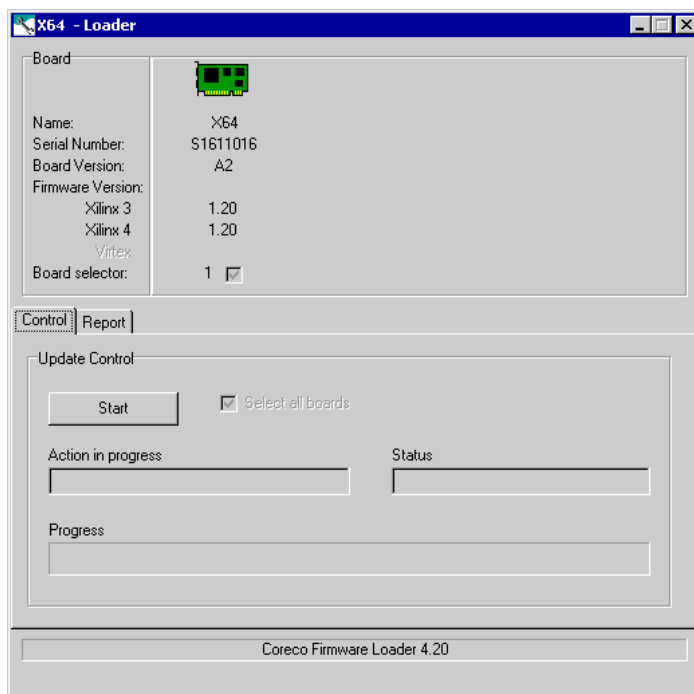


Choose a manual firmware upgrade when there are multiple X64 boards installed and a different firmware configuration is required for each board.

## Firmware Loader Status Window

The figure below shows the Firmware Loader program's status screen (with one X64-CL installed). Information on all installed X64-CL boards, their serial numbers, and their firmware components are shown. Additionally, a progress bar shows firmware programming status and a report tab lets the user view or print the firmware loader status report.

When selecting a manual firmware update, you choose which X64-CL will be reprogrammed via check boxes shown below each board (if there are multiple boards in the system).



---

Note: the Firmware Loader status report, generated from the Report tab, may be requested by Coreco Imaging Technical Support to aid in troubleshooting installation or operational problems.

---

## Executing the Firmware Loader from the Start Menu

If required, the X64-CL Firmware Loader program is executed via the Windows Start Menu shortcut **Start•Programs•Coreco Imaging•X64 Device Driver•Firmware Update**. Run the Firmware Loader when adding or changing X64 boards that do not have the current firmware.

---

# Enabling the CameraLink Serial Control Port

The CameraLink cabling specification includes a serial communication port for direct camera control by the frame grabber (see "J1: CameraLink Connector 1 (applies to X64-CL Dual & Full models)" [on page 83](#)). The X64-CL driver supports this serial communication port either directly or by mapping it to a host computer COM port. Any serial port communication program, such as Windows HyperTerminal, can connect to the camera in use and modify its function modes via its serial port controls.

---

Note: if your serial communication program can directly select the X64-CL serial port then mapping the X64-CL serial port to a system COM port is not necessary.

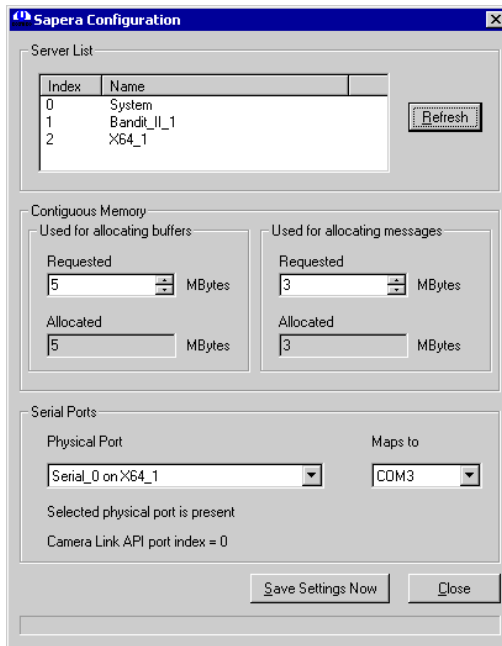
---

The X64-CL serial port is mapped to an available COM port by using the Sapera Configuration tool. Run the program from the Windows start menu: **Start•Programs•Coreco Imaging•Sapera LT•Sapera Configuration**.

## COM Port Assignment

The lower section of the Sapera Configuration program screen contains the serial port configuration menu. Configure as follows:

- Use the **Physical Port** drop menu to select the Sapera board device from all available Sapera boards with serial ports (when more than one board is in the system).
- Use the **Maps to** drop menu to assign an available COM number to that Sapera board serial port.
- Click on the **Save Settings Now** button then the **Close** button. You are prompted to reboot your computer to enable the serial port mapping.
- The X64-CL serial port, now mapped to COM3 in this example, is available as a serial port to any serial port application for camera control. Note that this serial port is not listed in the **Windows Control Panel•System Properties•Device Manager** because it is a logical serial port mapping.
- An example setup using Windows HyperTerminal follows (see "Setup Example with Windows HyperTerminal" [on page 17](#)).



The image shows a 'Sapera Configuration' window with three main sections: 'Server List', 'Contiguous Memory', and 'Serial Ports'. The 'Server List' section contains a table with three rows: '0 System', '1 Bandit\_IL\_1', and '2 X64\_1', with a 'Refresh' button to the right. The 'Contiguous Memory' section has two sub-sections: 'Used for allocating buffers' and 'Used for allocating messages'. Each sub-section has 'Requested' and 'Allocated' fields in MB, with spinners and 'MBytes' labels. The 'Serial Ports' section has a 'Physical Port' dropdown set to 'Serial\_0 on X64\_1', a 'Maps to' dropdown set to 'COM3', and status text indicating the port is present and the API port index is 0. At the bottom are 'Save Settings Now' and 'Close' buttons.

Index	Name
0	System
1	Bandit_IL_1
2	X64_1

Refresh

Contiguous Memory

Used for allocating buffers

Requested: 5 MBytes

Allocated: 5 MBytes

Used for allocating messages

Requested: 3 MBytes

Allocated: 3 MBytes

Serial Ports

Physical Port: Serial\_0 on X64\_1

Maps to: COM3

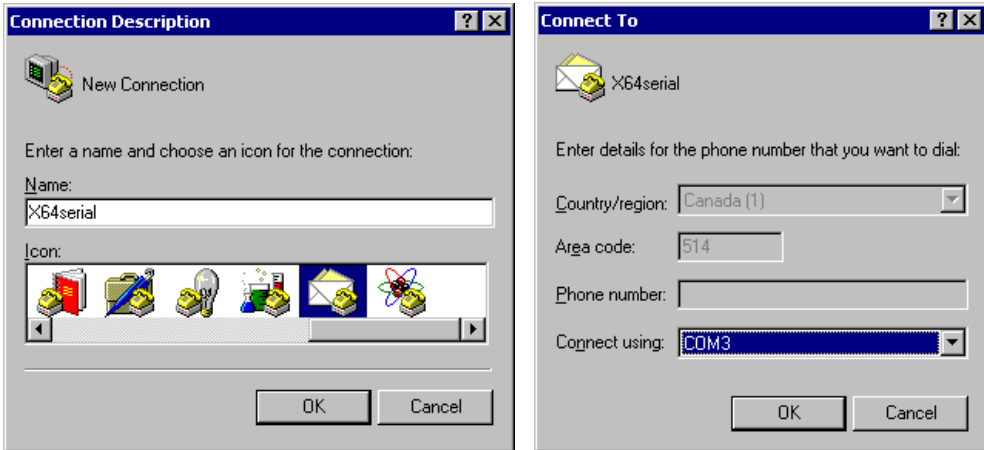
Selected physical port is present

Camera Link API port index = 0

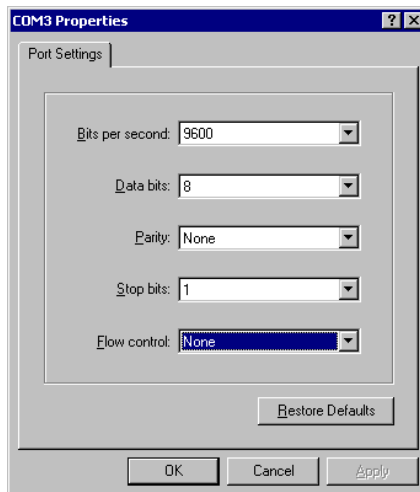
Save Settings Now Close

## Setup Example with Windows HyperTerminal

- Run HyperTerminal and type a name for the new connection when prompted. Then click OK.
- On the following dialog screen select the COM port to connect with. In this example the X64-CL serial port was previously mapped to COM3 by the Sapera Configuration program.



- HyperTerminal now presents a dialog to configure the COM port properties. Change settings as required by the camera you are connecting to. Note that the X64-CL serial port does not support hardware flow control.



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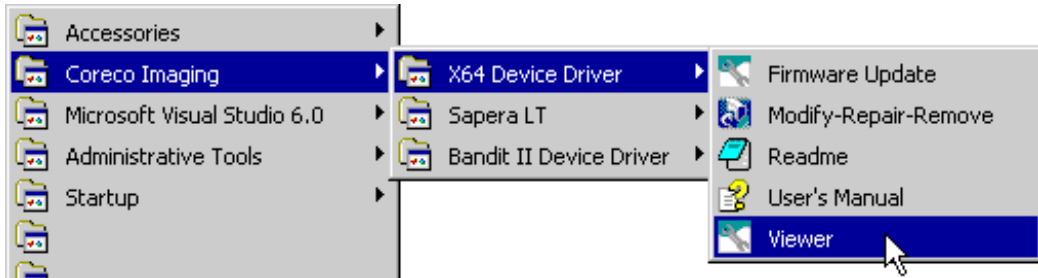
# Displaying X64-CL Board Information

The X64-CL Viewer program displays information about the X64-CL installed and its firmware revision.

---

Note: the X64-CL Viewer report generated by the **Save Board Info** button may be requested by Coreco Imaging Technical Support to aid in troubleshooting installation or operational problems.

---

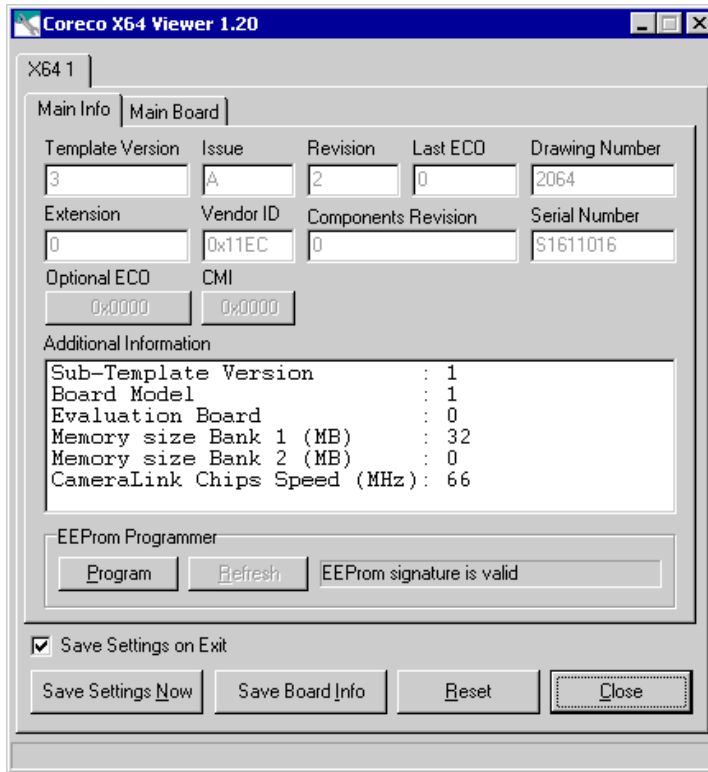


Run the X64-CL Viewer program from the X64 device driver start menu.

## X64-CL Viewer Windows

If multiple X64-CL boards are installed, each one is represented by a different 1st level dialog tab.

Buttons located at the bottom of the window are common for all sub-tabs. The **Save Settings Now** button stores the file path of custom firmware components manually installed (as described in following sections on the accompanying sub-tabs). The **Save Settings on Exit** check box performs similarly when the Viewer program is closed. The **Save Board Info** button saves all board information into a text file. Finally, the **Reset button** allows you to reset the board currently selected. Close all Sapera applications using resources from the board before resetting it.



## Main Info

For each X64-CL board, the **Main Info** tab displays information relating to the X64-CL board issue, revision, and ECO (engineering change order) level, along with the board serial number and optional ECO or CMI (customer modification instruction) applied.

The **Additional Information** window displays supplemental design data about the X64-CL. Note that **Board Model = 1** is the X64-CL Full and **Board Model = 2** is the X64-CL Dual.

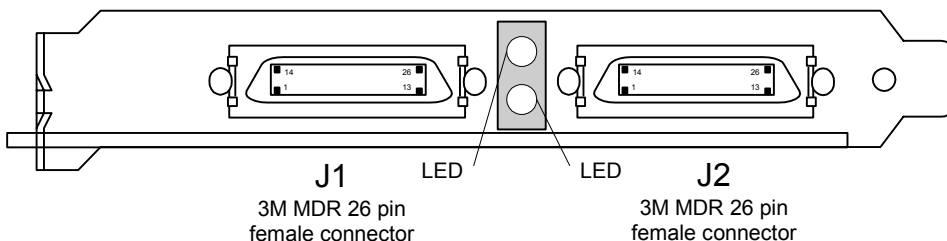
## Main Board

The **Main Board/Info** tab displays information relating to the X64-CL onboard firmware. The scroll window named **Content** provides firmware details such as version, release date, etc.

---

# Camera to CamLink Connections

## X64-CL Full / Dual



The hardware installation process is completed with the connection of a supported camera to the X64-CL board using CameraLink cables (see “CameraLink Cables” on page 99).

- The **X64-CL Full** board supports a camera with one or two CameraLink MDR-26 connectors (Base or medium or Full – see “Data Port Configuration Table” on page 98 for information on CameraLink configurations).
  - Connect the camera to the X64-CL J1 connector with a CameraLink cable. When using Medium or Full cameras, connect the second camera connector to X64-CL J2.
- The **X64-CL Dual** supports one or two Base CameraLink cameras.
  - Connect the first camera to the X64-CL J1 connector with a CameraLink cable. If using a second camera, connect to X64-CL J2.

Refer to section “Connector and Switch Specifications” on page 81 for details on the CameraLink connectors and the optional 12 pin Hirose connector.

---

Caution: If the camera is powered by the X64-CL via the Hirose connector or I/O connector block, it is very important that the correct power supply voltage is selected correctly. Refer to “J8 (CL), J12 (CL EM): Power to Camera Voltage Selector” on page 93 for information on the selection jumper.

---

Contact Coreco Imaging or browse our web site <http://www.imaging.com/camsearch> for the latest information on X64-CL supported cameras.

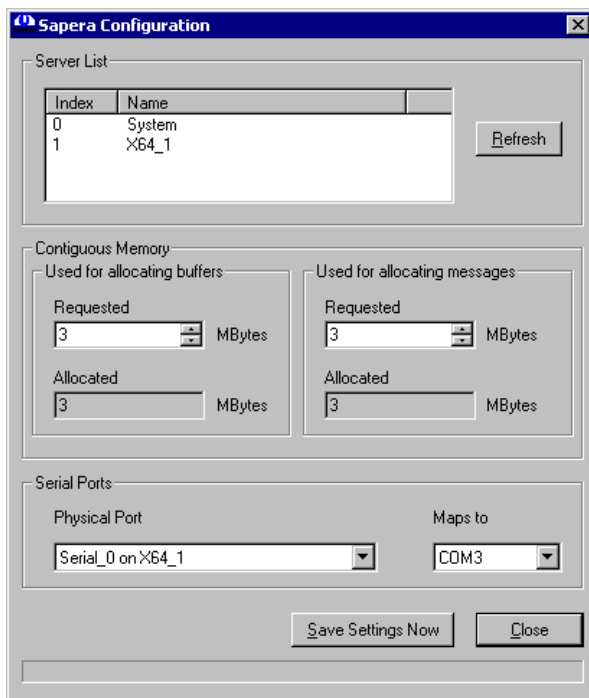
---

# Configuring Sapera

## Viewing Installed Sapera Servers

The Sapera configuration program (**Start•Programs•Coreco Imaging•Sapera LT•Sapera Configuration**) allows the user to see all available Sapera servers for the installed Sapera-compatible boards.

The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should always be present. As shown in the following screen image, server index 1 is the X64-CL board installed. If required, update the server list by clicking the **Refresh** button.



## Increasing Contiguous Memory for Sapera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory, occupying consecutive addresses) reserved for the resources needed for **Sapera buffers** allocation and **Sapera messaging**. For both items, the **Requested** value dialog box shows the driver default memory setting while the **Allocated** value displays the amount of contiguous memory that has been allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sapera buffers** value determines the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for host frame buffer management such as DMA descriptor

tables plus other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers. You can approximate the amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for frame buffers  
( number of frame buffers • number of pixels per line • number of lines • (2 - if buffer is 10 or 12 bits) ).
- Provide 1MB for every 256 MB of host frame buffer memory required.
- Add an additional 1 MB if the frame buffers have a short line length, say 1k or less  
( the increased number of individual frame buffers requires more resources ).
- Add an additional 2 MB for various static and dynamic Sopera resources.
- Test for any memory error when allocating host buffers. Simply use the "General Options" on page 44 Buffer menu of the Sopera Grab demo program (see "Using the Grab Demo" on page 41) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum limit of host buffers possible on your host system – the Sopera Grab demo will not crash when the requested number of host frame buffers cannot be allocated.

## Host Computer Frame Buffer Memory Limitations

When planning a Sopera application and its host frame buffers used, plus other Sopera memory resources, do not forget the Windows operating system memory needs. Window XP as an example, should always have a minimum of 128 MB for itself.

A Sopera application using *scatter gather buffers* could consume most of the remaining system memory. When using frame buffers allocated as a *single contiguous memory block*, typical limitations are one third of the total system memory with a maximum limit of approximately 100 MB. See the "General Options" on page 44 Buffer menu of the Sopera Grab demo program for information on selecting the type of host buffer memory allocation.

## Contiguous Memory for Sopera Messaging

The current value for **Sopera messaging** determines the total amount of contiguous memory reserved at boot time for messages allocation. This memory space is used to store arguments when a Sopera function is called. Increase this value if you are using functions with large arguments, such as arrays and experience any memory errors.



# CamExpert Quick Start for the X64-CL

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## Interfacing Cameras with CamExpert

CamExpert is the camera interfacing tool for frame grabber boards supported by the Sapera library. CamExpert generates the Sapera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. For backward compatibility with previous versions of Sapera, CamExpert also reads and writes the \*.cca and \*.cvi camera parameter files.

An important component of CamExpert is its live acquisition display window which allows immediate verification of timing or control parameters without the need to run a separate acquisition program.

For context sensitive help click on the  button then click on a camera configuration parameter. A short description of the configuration parameter will be shown in a popup. Click on the  button to open the help file for more descriptive information on CamExpert.

---

## Overview of this Example: Interfacing the Piranha2 Linescan

The CamExpert utility is presented by using the example of interfacing the Dalsa Piranha2 Linescan camera. The major steps covered are:

- Sapera camera control files, new and legacy format
- Camera interfacing check list
- CamExpert interfacing outline
- Piranha2 in free run exposure mode
- Piranha2 in external exposure mode
- Piranha2 with shaft encoder line sync, using fixed or variable frame buffers

---

## Camera Types & Files Applicable to the X64-CL

The X64-CL supports digital area scan or linescan cameras using the CameraLink interface standard. See "Camera to CamLink Connections" on page 20 for information on connecting a CameraLink camera to either the X64-CL Full or X64-CL Dual frame grabber.

Contact Coreco Imaging or browse our web site [ <http://www.imaging.com/camsearch> ] for the latest information and application notes on X64-CL supported cameras.

## Camera Files Distributed with Sopera

The Sopera distribution CDROM includes camera files for a selection of X64-CL supported cameras. Using the Sopera CamExpert program, you may use the camera files (CCA) provided to generate a camera configuration file (CCF) that describes the desired camera and frame grabber configuration..

Coreco Imaging continually updates a camera application library composed of application information and prepared camera files. Along with the camera search utility on the Coreco Imaging web site, as described above, a number of camera files are ready to download from the Coreco Imaging FTP site [[ftp://ftp.coreco.com/public/Sopera/CamFile\\_Updates](ftp://ftp.coreco.com/public/Sopera/CamFile_Updates)]. Camera files are ASCII text and can be read with Windows Notepad on any computer without having Sopera installed.

## CamExpert Memory Errors when Loading Camera Configuration Files

The memory error message [ **Error: "CorXferConnect" <Xfer module> - No memory ()** ] may occur when loading a Sopera camera file, or when the application configures a frame buffer for area scan cameras. The problem is that the X64-CL does not have enough onboard memory for two frame buffers.

The X64-CL when used with area scan cameras, allocates two internal frame buffers in onboard memory, each equal in size to the acquisition frame buffer. This allocation is automatic at the driver level. The X64-CL driver allocates two buffers to ensure that the acquired video frame is complete and not corrupted in cases where the transfer to host system memory may be interrupted by other host system processes.

The total size of the two internal frame buffers must be somewhat smaller than the total onboard memory due to memory overhead required for image transfer management. Also note that the X64-CL Dual board equally divides the onboard memory between the two acquisition modules, reducing the available memory for the two buffers by half.

## Overview of Sopera Acquisition Parameter Files (\*.ccf or \*.cca/\*.cvi)

### Concepts and Differences between the Parameter Files

There are two components to the legacy Sopera acquisition parameter file set: CCA files (also called cam-files) and CVI files (also called VIC files, i.e. video input conditioning). The files store video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplifies programming the frame-grabber acquisition hardware for the camera in use. **Sopera LT 5.0** introduces a new camera configuration file (CCF) that combines the CCA and CVI files into one file.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera operating mode). An application can also have multiple CCA/CCF files so as to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

## CCF File Details

Files using the “.CCF” extension, (CORECO Camera Configuration files), are essentially the camera (CCA) and frame grabber (CVI) parameters grouped into one file for easier configuration file management. This is the default Camera Configuration file used with Sapera LT 5.0 and the CamExpert utility.

## CCA File Details

Coreco Imaging distributes camera files using the “.CCA” extension, (CORECO CAMERA files), which contain all parameters describing the camera video signal characteristics and operation modes (what the camera outputs). The Sapera parameter groups within the file are:

- Video format and pixel definition.
- Video resolution (pixel rate, pixels per line, lines per frame).
- Synchronization source and timing.
- Channels/Taps configuration.
- Supported camera modes and related parameters.
- I/O hardware signal assignment.

## CVI File Details

Legacy files using the “.CVI” extension, (CORECO VIDEO files), contain all operating parameters related to the frame grabber board - what the frame grabber can actually do with camera controls or incoming video. The Sapera parameter groups within the file are:

- Activate and set any supported camera control mode or control variable.
- Define the integration mode and duration.
- Define the strobe output control.
- Allocate the frame grabber transfer ROI, the host video buffer size and buffer type (RGB888, RGB101010, MONO8, MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, LVDS, OPTO-isolated), and signal active edge or level characterization.

## Camera Interfacing Check List

Before undertaking the task of interfacing a camera from scratch with CamExpert:

- Confirm that Coreco Imaging has not already published an application note with camera files [<http://www.imaging.com/camsearch>].
- Confirm that Sapera does not already have a .cca file for your camera installed on your hard disk. If there is a .cca file supplied with Sapera, then use CamExpert to automatically generate the .ccf file with default parameter values matching the frame grabber capabilities.

- Check if the Sapera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert where it is modified to match timing and operating parameters for your camera, and lastly save them as Camera Configuration file (.ccf), or as a new .cca & .cvi camera file pair for applications built with Sapera 4.2 or earlier.
- Finally, if your camera type has never been interfaced, run CamExpert after installing Sapera and the acquisition board driver, select the board acquisition server, and enter the camera parameters.

---

## Linescan Example: Interfacing the Dalsa Piranha2 Linescan Camera

These examples use a X64-CL Full board connected to the Piranha2 CameraLink camera (P2-2x or P2-4x). The model P2-4x 06k, a 4 tap 40 MHz 6k pixel digital linescan camera was used for the CamExpert screen shots. Download the user's manual directly from the Dalsa web site <http://www.dalsa.com/>.

### CamExpert Interfacing Outline

- Sapera and the X64-CL device driver are installed as described in this manual.
- Check for an existing CCA file, distributed with Sapera, that will provide camera timing parameters.
- Check the Coreco Imaging web site for a published application note with camera files [<http://www.imaging.com/camsearch>].
- Connect two (for this example) CameraLink interface cables between the X64-CL and camera. Connect power to the camera.
- Run Windows HyperTerminal and establish communication with the camera. Verify the camera's settings (the Dalsa command to return all camera parameters is `get_camera_parameters`).
- Set the camera to its free run mode or its self generated test pattern. This will simplify testing the camera file timing parameters.
- Run CamExpert, load or set camera timing parameters and capabilities, and then test a live grab. Save the camera file for the default free run mode.
- Using HyperTerminal, set the camera to external sync and external line integration mode.
- Configure CamExpert for camera external sync with external line integration control. Test variations in line rate and integration period. Save a new camera file when satisfied.

---

## step 1: Piranha2 in Free Run Exposure Mode

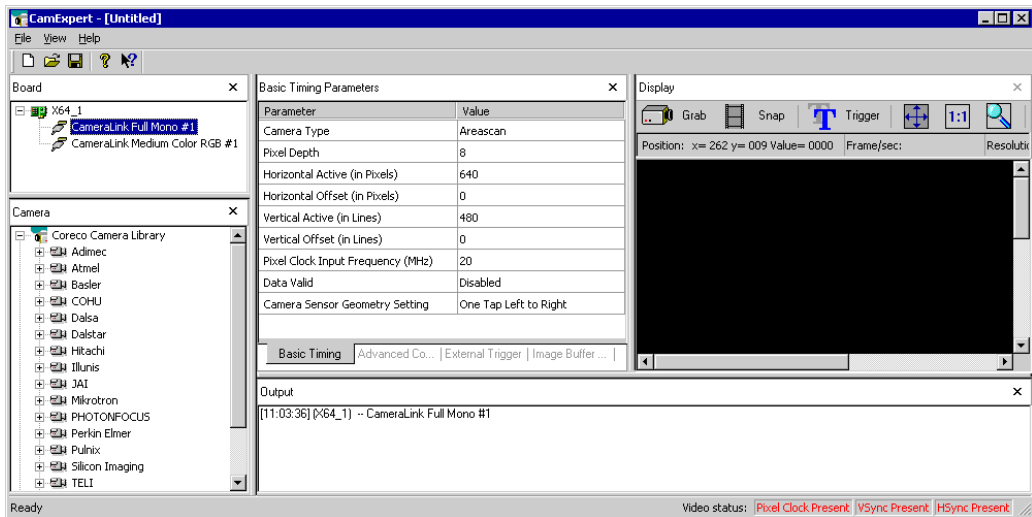
This section illustrates the CamExpert dialog screens for interfacing the Dalsa Piranha2 in free run mode. Dalsa defines this exposure mode as where the camera uses its internal SYNC and PRIN, at a maximum line rate and exposure time. This is the Piranha2 factory default mode and serves well as a CamExpert interfacing example.

To verify or set the Piranha2 in free run mode:

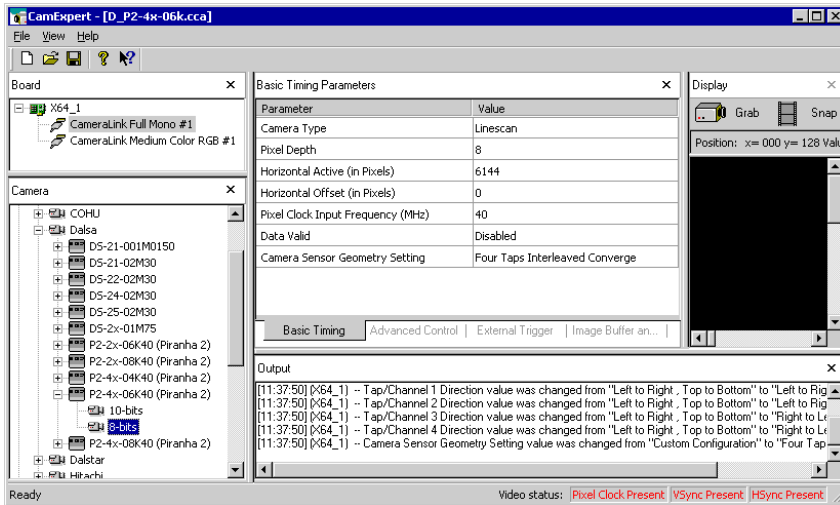
- With HyperTerminal type the Dalsa command to return the camera parameters  
get\_camera\_parameters.
- Check the value for Exposure Mode, which is 2 for internal SYNC and PRIN.
- If the value is different, enter the command set\_exposure\_mode 2.

## File Selection & Grab Test

- From the Windows start menu run the Sapera CamExpert program.  
[Programs|Coreco Imaging|Sapera LT|CamExpert ]
- CamExpert opens with default settings for the X64-CL (assuming the X64-CL is the only Sapera frame grabber installed). In the **Board** window, click on the CameraLink Full Mono #1 acquisition server, as shown in the following screen image.



- The **Camera** window shows camera files distributed with Sapera that are supported by the X64-CL (Coreco Camera Library). The User's Configuration File section is the default location for \*.ccf files saved by CamExpert and also the default location that Sapera demo programs use to read camera configuration files.
- Select the Dalsa P2-4x 06k Piranha2 8-bit camera. The following screen image shows that CamExpert automatically loads the basic timing parameters from the distribution cca file.



- With the Piranha2 configured for internal sync and PRIN (free run mode), click the Grab button to have live acquisition in the display window. The camera may need to be pointed to a bright wall or light source.
- Refer to the CamExpert video **status bar** to see if any required timing signals are missing. Also check the X64-CL status LEDs (see "Status LEDs Functional Description" on page 82) to aid in troubleshooting camera problems.
- This non-triggered exposure mode can be used to confirm a linescan inspection setup if the speed of the object or web is varied to match the fixed camera exposure.
- Use the **File-Save** dialog to save this camera configuration file (\*.ccf) with user entered information. CamExpert provides information for each field based on the file originally loaded. Modify the fields such as camera mode and board configuration, to describe the parameter setup. Modify the file name and click Save. The ccf file is located in the default Sapera user folder. The screen image below is an example.

**Save Camera file**

Camera Configuration Description

Company Name: Dalsa

Model Name: P2-4x-06K40 (Piranha 2)

Camera Mode: 8-bits

Board Configuration: Internal-Sync&PRIN linescan

File Information

File name: D\_P2-4x-06K40\_(Piranha\_2)\_8-bits\_Internal-Sync&PR

Save as type: Camera configuration file (.ccf)

Current directory: C:\Coreco\Sapera\CamFiles\User

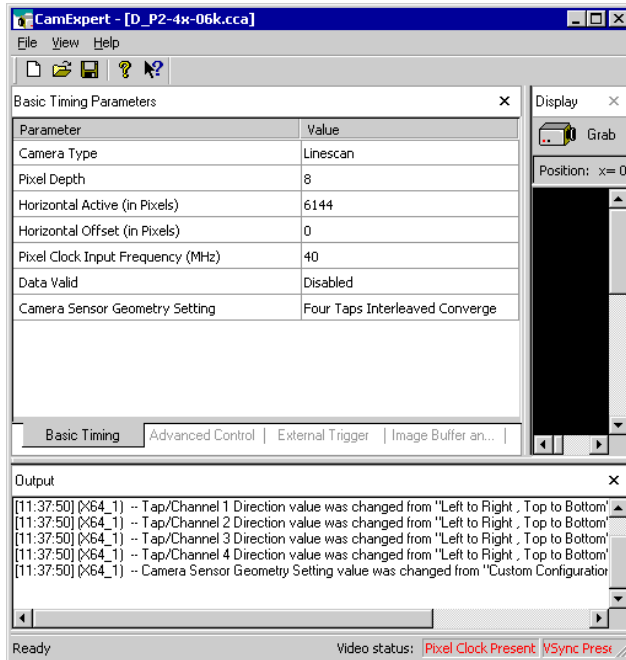
☐ Select Custom Directory Browse...

Save Cancel

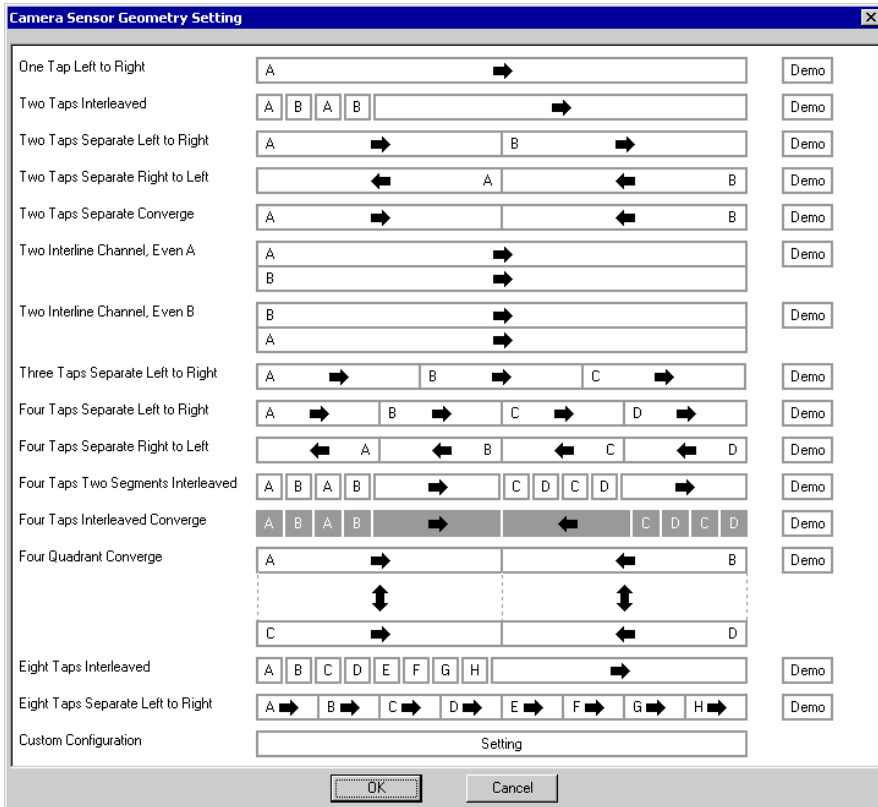
## Overview of Basic Timing Parameters

CamExpert only shows parameters applicable to the acquisition board and camera type. When configuring parameters for a new camera start by selecting or entering the basic horizontal timing parameters and pixel clock frequency as defined by the camera manufacturer.

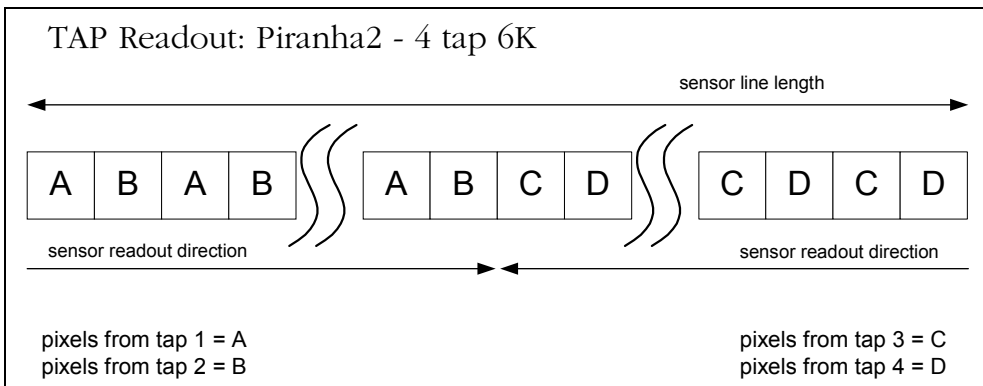
The following screen image shows the Basic Timing Parameters required for the X64-CL with a linescan camera (parameters are for the Piranha2 - P2-4x 06k 8-bit camera).



- Pixel Depth depends on the camera digital data. The Dalsa Piranha2 linescan camera digitizes internally to 10 bits and outputs either all 10 bits or the most significant 8 bits. When selecting 8 bits, the Sopera frame buffer required is 8 bit mono. When selecting 10 bit, the Sopera frame buffer required is 16 bit mono.
- Data Valid: Some CameraLink cameras use a data valid signal in addition to line valid and/or frame valid control signals. The Dalsa Piranha2 does not, therefore this selection is set to disable.
- For the **Camera Sensor Geometry** parameter select one from the many standards supported by the acquisition board, or the user defines a custom geometry. The following screen image shows the sensor geometry selection window for the X64-CL.



The Piranha2 model P2-4x 06k, 4 tap - 6k pixel camera uses a tap structure as shown in the next figure. Tap 1 and 2 are simultaneously readout from a left to right direction while taps 3 and 4 are readout from a right to left direction. The advantage of multiple tap cameras is that the pixel clock rate is kept reasonably low while the data output to the frame grabber is increased. A camera with more than one tap has a higher average bandwidth by simultaneously outputting separate portions of a single sensor exposure.



---

## step 2: Piranha2 in External Exposure Mode

Using the Piranha2 camera in external exposure (line integration) mode requires a few changes to both the camera's operating mode and the Piranha2 camera file used for free run exposure mode. The modified camera file should be given an appropriate description and saved with a unique file name.

Before using CamExpert to generate and test the modified camera file, set the Piranha2 camera to the desired external exposure mode as follows:

- With HyperTerminal type the Dalsa command `set_exposure_mode 5` to set the camera for external SYNC and PRIN control from the frame grabber. Acquisition and exposure will now be controlled by the X64-CL.
- The Piranha2 camera will respond with warnings that external SYNC and PRIN are not detected. This is normal since CamExpert has not yet been configured for line integration mode.

To simplify this example the X64-CL will generate the line sync trigger. The X64-CL is programmed for the line trigger frequency and line integration method matching the Piranha2 specifications.

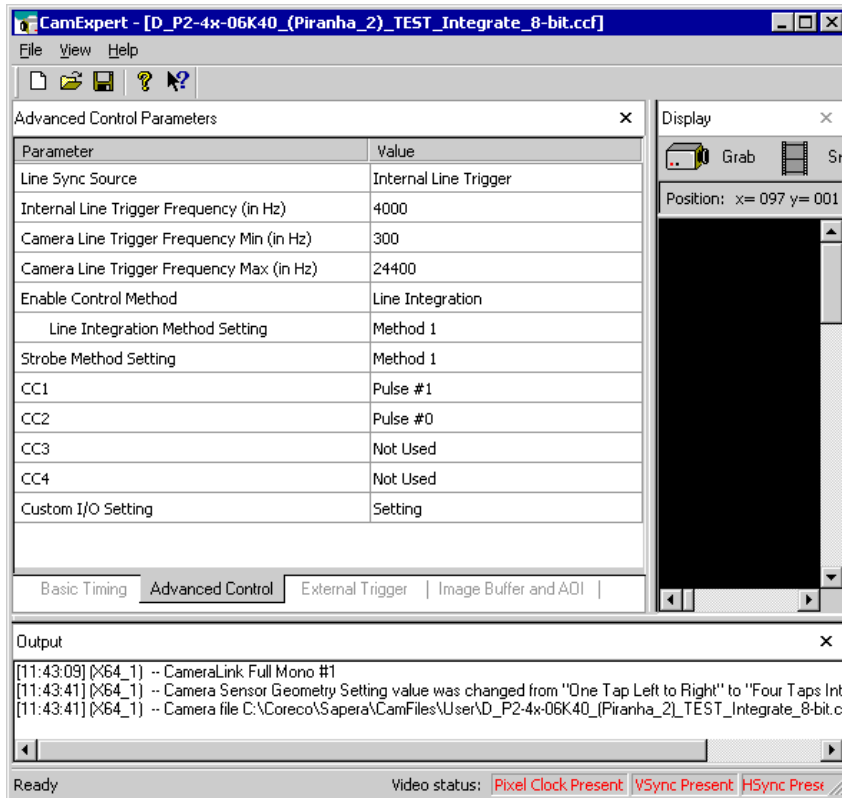
### CCF File Selection

To configure this new CCF file, start by loading the CCF for free run mode from the previous section.

- From the Windows start menu run the Spera CamExpert program.  
[Programs|Coreco Imaging|Spera LT|CamExpert ]
- In the **Board** window, click on the CameraLink Full Mono #1 acquisition server.
- From the **Camera** file selection window, select the ccf camera file previously saved for the Piranha2 in free run exposure mode, as configured in the previous section "step 1: Piranha2 in Free Run Exposure Mode" [on page 26](#).

### Advanced Control Parameters

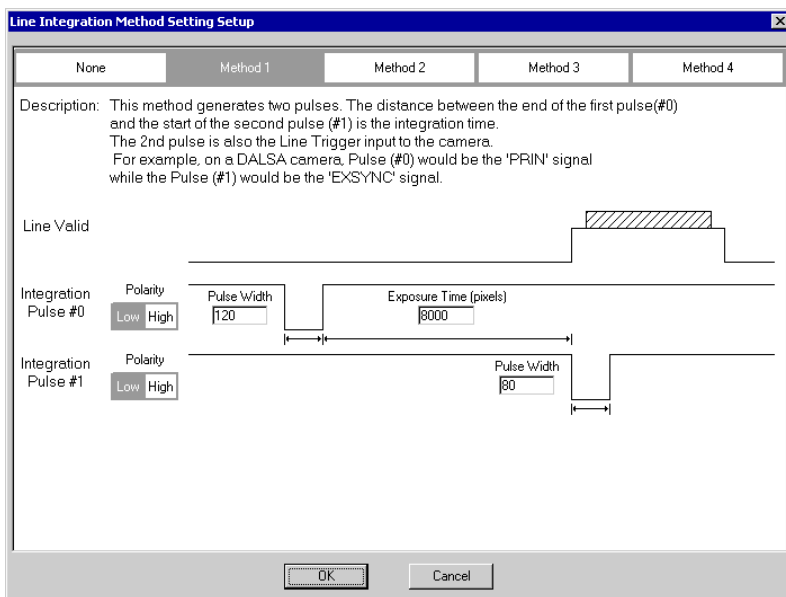
The CamExpert advanced control parameters tab, as shown in the following screen image, contains the configuration items needed for external trigger and exposure control. Descriptions of each parameter, as setup for this example with the Piranha2, follow the screen image.



- **Line Sync Source:** Set to internal line trigger. The X64-CL will generate the camera line trigger without using an external event or trigger.
- **Internal Line Trigger Frequency:** Set the line rate generated by the X64-CL. The line sync rate is set to 4 kHz which is a period of 250 $\mu$ s. This period must be longer then the combined PRIN control pulse time (active low for pixel reset) and the integration time (time between rise of PRIN to EXSYNC). These control signals are described below.
- **Camera Line Trigger Frequency Min & Max:** Set to the camera specification limits so that CamExpert can trap invalid entries.
- **Enable Control Method:** Line Integration is selected as the required control mode.
- **Line Integration Method Setting and CameraLink Control Signals CC1-CC4:** The CameraLink CC1 and CC2 controls are assigned to Sapera controls which are not very descriptive by themselves. These selections are dependent on the camera's control specifications. The required camera controls are matched to the corresponding Sapera exposure method. The logical sequence to set these parameters is as follows.
  - From the Piranha2 user manual, the required CameraLink camera control configuration is **CC1 = EXSYNC** and **CC2 = PRIN**.
  - From the Piranha2 user manual, note the timing requirements for external EXSYNC and PRIN. PRIN specifies a minimum logic low time for pixel reset which must be

respected. When PRIN is logic high, the camera is integrating. Following an integration period the falling edge of EXSYNC triggers the line readout.

- Review the Spera integration methods for a two pulse control which matches the camera control specifications. The Spera Line Integration Method #1 matches the control requirement. See "Line Integration Method #1" on page 54 for a timing illustration.
- From this information, it is seen that PRIN (CC2) corresponds to the Spera control Pulse #0 and EXSYNC (CC1) corresponds to Spera control Pulse # 1. Set the CamExpert camera controls to match these requirements. Note that CameraLink controls CC3 and CC4 are not used by the Piranha2.
- Click on the line integration method setting field. A configuration window allows selecting a method number corresponding to the Spera integration methods.
- Select method 1. Configure the control pulses for polarity and signal width as shown in the following screen image. Descriptions for these parameters follow.



- For Pulse #0 (assigned to PRIN), select polarity and width. The Piranha2 specifies that PRIN must be a minimum  $2\mu\text{s}$  active low pulse. At a 40Mhz pixel clock, 40 pixels equal  $1\mu\text{s}$ , thus a setting of 120 pixels generates a  $3\mu\text{s}$  PRIN. Note that the X64-CL on-board pulse generator works in increments of 1 $\mu\text{s}$ .
- Knowing that 40 pixels is  $1\mu\text{s}$ , this example sets an integration time of 8000 pixels which is  $200\mu\text{s}$ . This value must be less then the line trigger rate which was set to 4 KHz ( $250\mu\text{s}$ ).
- For Pulse #1 (assigned to EXSYNC), select polarity and width. In this example EXSYNC is active low for 2  $\mu\text{s}$  (80 pixels).

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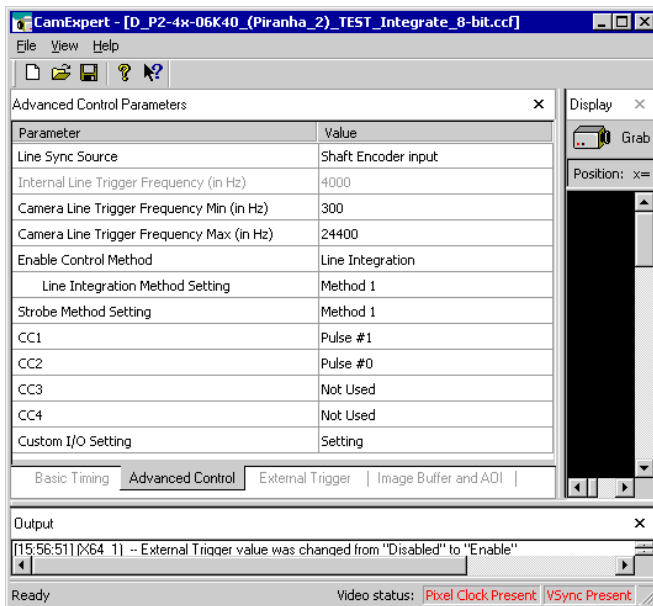
## step 3: Piranha2 with Shaft Encoder Line Sync

Continuing from the previous setup ("step 2: Piranha2 in External Exposure Mode" on page 32), this section details using the X64-CL shaft encode inputs as the exposure trigger for the imaging system. In addition the virtual frame reset feature is used to have an n number of image lines grabbed into the Sapera frame buffer when triggered by some external event.

- See "Shaft Encoder Interface Timing" on page 50 for an overview of the quadrature shaft encoder supported by the X64-CL, and the I/O connections used.
- See "Virtual Frame\_Reset for Linescan Cameras" on page 51 for an overview of using an external frame reset signal to initiate the acquisition of n number of lines, and the I/O connections used.

### Shaft Encoder Line Sync Setup

- Assuming the same PRIN and EXSYNC timing from the previous example, on the Advanced Control Parameters tab, the **Line Sync Source** signal Shaft Encoder is now selected.

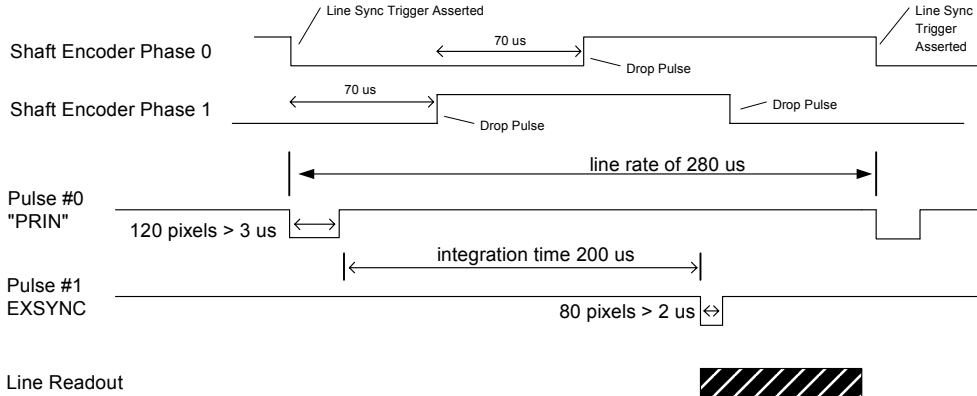


- This example uses a line integration time of 200 $\mu$ s therefore the line sync source must have a period greater then the integration time plus the PRIN duration.
- Assuming quadrature shaft encoder signals every 70 $\mu$ s, by dropping three out of every four pulses, a line sync occurs every 280 $\mu$ s. The following timing diagram (not to scale) illustrates the shaft encoder signals relative to PRIN and EXSYNC.

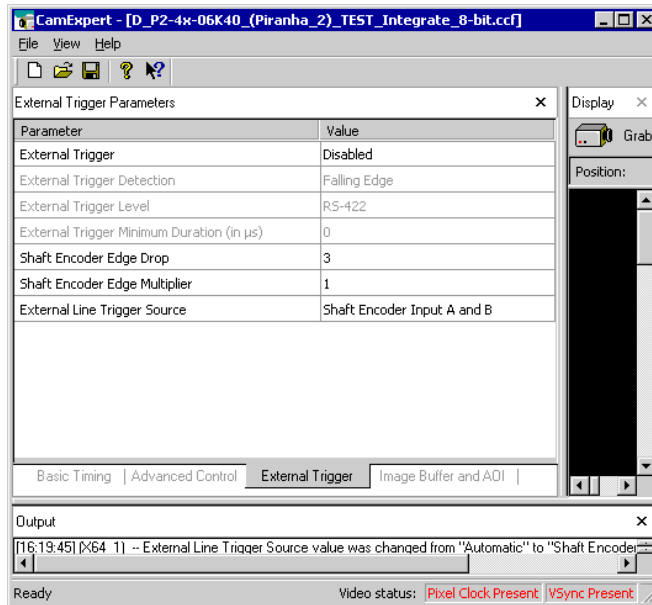
## Piranha2 External Exposure with Shaft Encoder Line Sync Control

This simple example drops 3 of every 4 quadrature shaft encoder pulse edges.

Note: Timing shown is not to scale.



- Select the CamExpert **External Trigger Parameters** tab. The External Line Trigger Source is set to use both shaft encoder inputs. The edge drop factor is set to 3 to match the example timing diagram shown above.

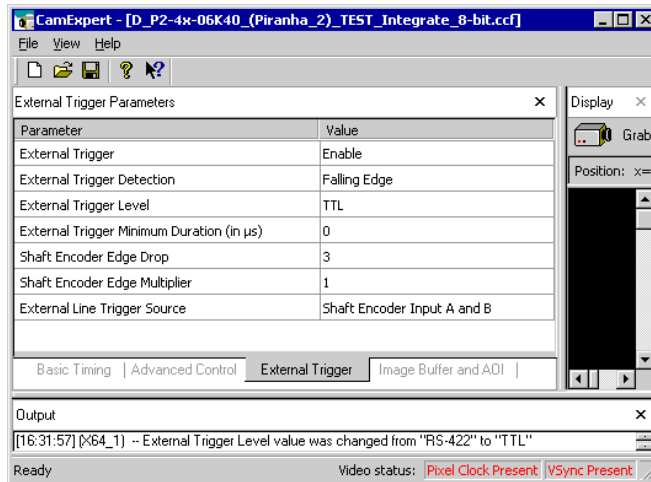


Using shaft encoder signals only, the X64-CL grabs linescan data continuously into a memory frame buffer. The number of data lines stored (i.e. the vertical size of this frame buffer – see the Image Height

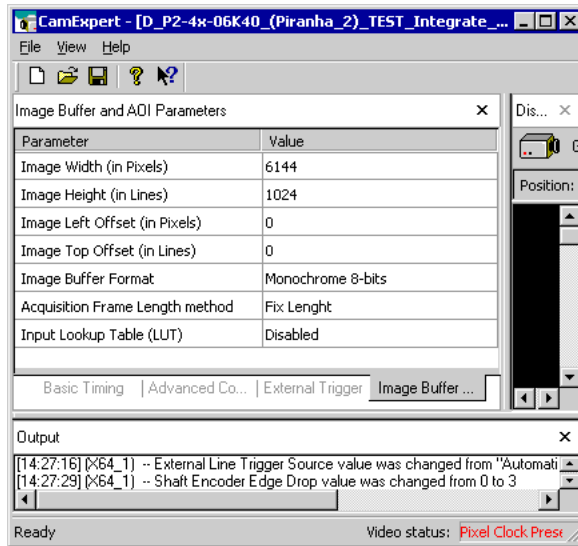
parameter on the Image Buffer tab) is arbitrarily set by the user. With continuous shaft encode signals, after the frame buffer is filled with captured data lines, new data lines will then overwrite previous data.

## Shaft Encoder with Fixed Frame Buffer Setup

To synchronize the capture of linescan data, an external trigger signal input to the X64-CL is used to start acquisition into the frame buffer. In this example, when the external trigger is asserted, the X64-CL then triggers linescan data captures based on the shaft encoder inputs. When the frame buffer is filled, linescan capture is suspended until the next external trigger. Example screen images of the External Trigger Parameters and the Image Buffer Parameters tabs follow.



- **External Trigger:** Set to Enable
- **External Trigger Detection:** Select which pulse edge or from a level active trigger. Available choices are dependent on the acquisition board used.
- **External Trigger Level:** Choose the signal type connect as an external trigger.



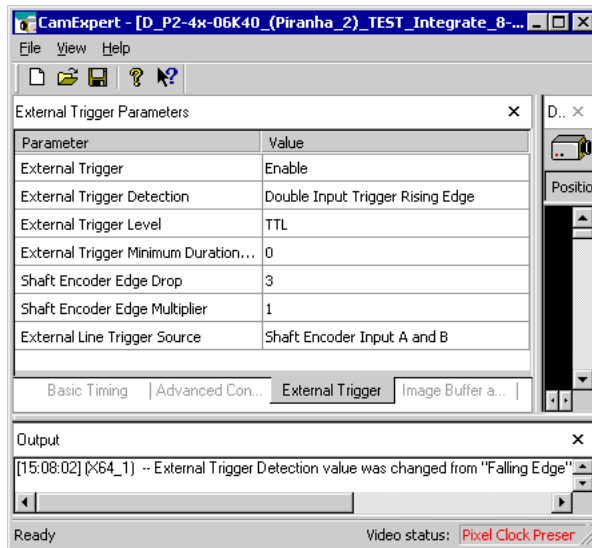
- **Image Width:** By default the buffer is the same as the acquisition width.
- **Image Height:** Set to the maximum number of acquired lines needed. Refer to the hardware specifications for the maximum limit.
- **Acquisition Frame Length method:** In this example, set to fixed length when there is a single trigger signal to start the acquisition of one complete frame buffer.

Assuming that the shaft encoder and external trigger signals are connected (refer to "I/O Connector Bracket Assembly" on page 89), click on Grab to test the linescan camera setup.

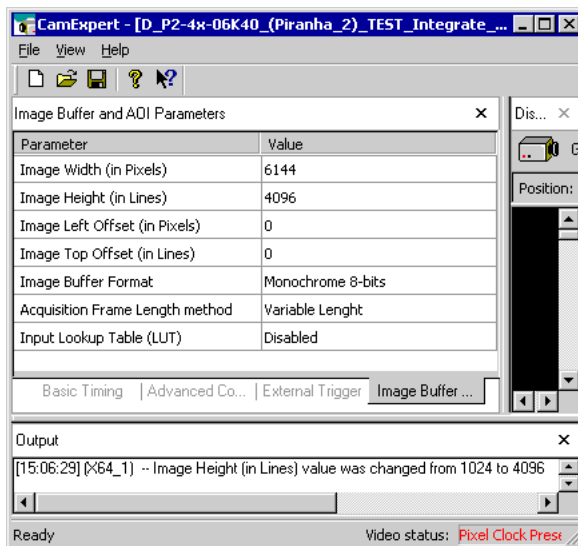
## Shaft Encoder with Variable Frame Buffer Setup

To synchronize the capture of a variable amount of linescan data, external trigger signals input to the X64-CL are used to start and stop line acquisition into the frame buffer. The grab control can either be a level type (where the acquisition occurs while the external control is active high), or the grab control can be a two pulse trigger (where trigger pulse 1 starts the line acquisition and trigger pulse 2 stops acquisition).

The actual linescan data capture is still triggered by the shaft encoder inputs. If the frame buffer is filled before the stop acquisition trigger control occurs, the linescan capture is suspended until the next start acquisition trigger. Example screen images of the External Trigger Parameters and the Image Buffer Parameters tabs follow.



- **External Trigger:** Set to Enable
- **External Trigger Detection:** In this example trigger input 1 starts the linescan acquisition and trigger input 2 ends the acquisition. The number of lines is variable.
- **External Trigger Level:** Choose the signal type connect as an external trigger.



- **Image Width:** By default the buffer is the same as the acquisition width.
- **Image Height:** Set to the maximum number of acquired lines needed. Refer to the hardware specifications for the maximum limit.
- **Acquisition Frame Length method:** In this example, set to variable length when there is both a start trigger pulse and an end trigger pulse to control the acquisition into the frame buffer. A level trigger signal (active high period or active low period) is also used for a grab controller with a variable length frame buffer.

Assuming that the shaft encoder and external trigger signals are connected (refer to "I/O Connector Bracket Assembly" on page 89), click on Grab to test the linescan camera setup.

# The Sopera Demo Application

---

## Grab Demo Overview

<b>Program</b>	<b>Start•Programs•Sopera LT•Demos•Grab Demo</b>
<b>Program file</b>	<b>\Coreco\Sopera\Demos\Classes\vc\GrabDemo\Release\GrabDemo.exe</b>
<b>Workspace</b>	<b>\Coreco\Sopera\Demos\Classes\vc\SapDemos.dsw</b>
<b>Description</b>	This program demonstrates the basic acquisition functions included in the Sopera library. The program allows you to acquire images, either in continuous or in one-shot mode, while adjusting the acquisition parameters. The program code may be extracted for use within your own application.
<b>Remarks</b>	This demo is built using Visual C++ 6.0 using the MFC library. It is based on the Sopera standard API and Sopera C++ classes. See the Sopera User's and Reference manuals for more information.

## Using the Grab Demo

### Server Selection

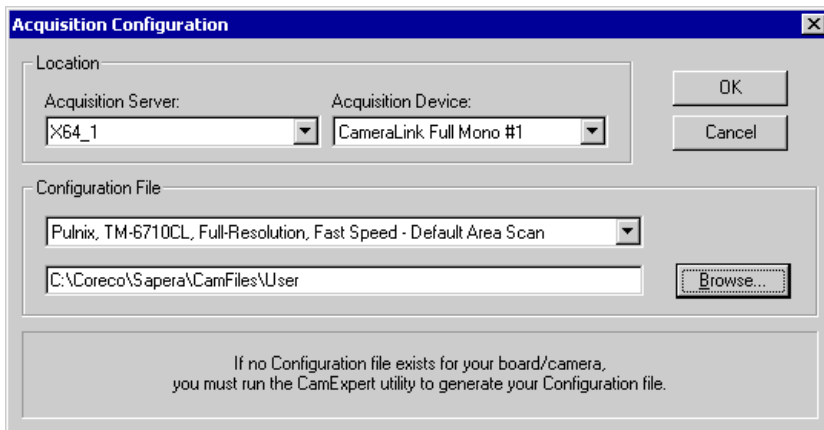
Run the grab demo from the start menu **Start•Programs•Sopera LT•Demos•Grab Demo**.

The demo program first displays the acquisition configuration menu. The first drop menu displayed permits selecting from any installed Sopera acquisition servers (installed Coreco Imaging acquisition hardware using Sopera drivers). The second drop menu permits selecting from the available input devices present on the selected server.

### CCF File Selection

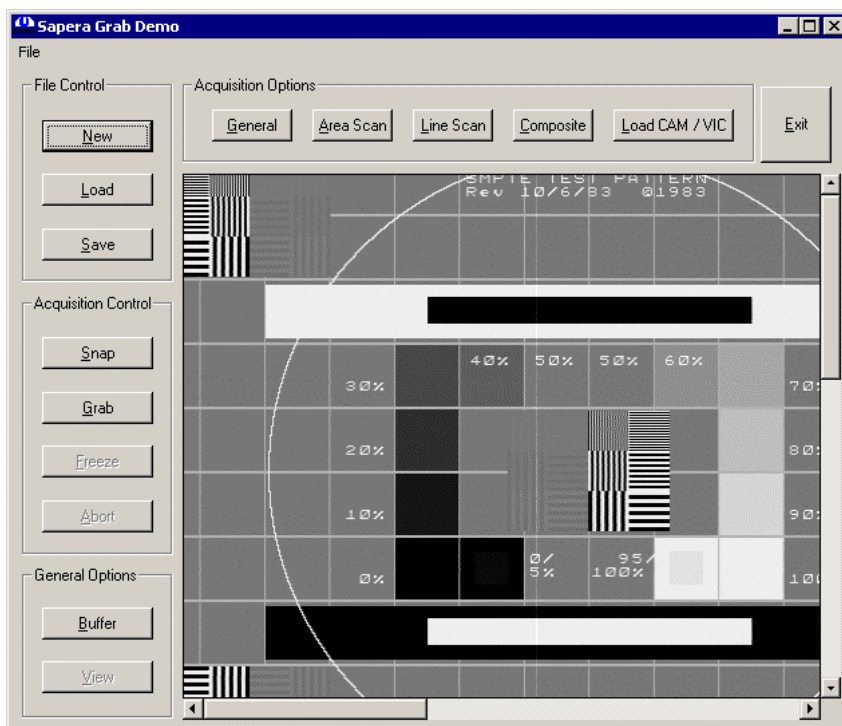
The acquisition configuration menu is also used to select the required camera configuration file for the connected camera. Sopera camera files contain timing parameters and video conditioning parameters. The default folder for camera configuration files is also used by the CamExpert utility to save user generated or modified camera files.

Use the Sopera CamExpert utility program to generate the camera configuration file based on timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of those parameters. CamExpert reads both Sopera \*.cca and \*.cvi for backward compatibility with the original Sopera camera files.



## Grab Demo Main Window

The demo main window provides control buttons and a central area for displaying the grabbed image. Developers can use the demo source code as a foundation to quickly create and test the desired imaging application.



The following sections describe the various functions:

## File Control

Three controls are provided for image file transfers.

- **New:** Clear the current image frame buffer.
- **Load:** Retrieves images in BMP, TIF, CRC, JPG, and RAW formats.
- **Save:** Prompts for a file name, file save location, and image format.

## Acquisition Options

---

Note that unsupported functions are grayed out and not selectable. Function support is dependent on the frame grabber hardware in use.

---

- **General – Acquisition Settings:** Allows enabling X64-CL external trigger mode.
- **Area Scan – Camera Control:** Provides trigger, reset, and integrate control when supported by the current hardware and driver.
- **Line Scan – Camera Control:** Provides linescan camera controls such as external line/frame trigger selection, shaft encoder input selection, etc. when supported by the current hardware and driver.
- **Composite - Conditioning:** This dialog is not applicable to the X64-CL.
- **Load CAM/VIC:** Opens the dialog window **Acquisition Parameters** allowing the user to load a new set of camera files. This is the same window as when the Spera Acquisition demo is started.

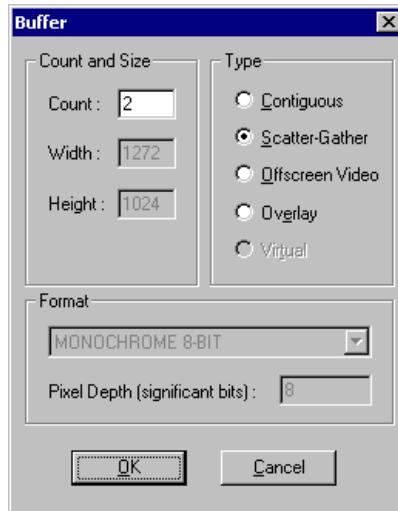
## Acquisition Control

- **Grab:** See live digitized video from your video source. If your source is a camera, focus and adjust the lens aperture for the best exposure. Use a video generator as a video source to acquire reference images.
- **Freeze:** Stop live grab mode. The grabbed image can be saved to disk via the **File Control•Save** control.
- **Snap:** A single video frame is grabbed.
- **Abort:** Exits the current grab process immediately. If any video signal problem prevents the freeze function from ending the grab, click on the **Abort** button.

## General Options

Note: functions grayed out are not supported by the acquisition hardware.

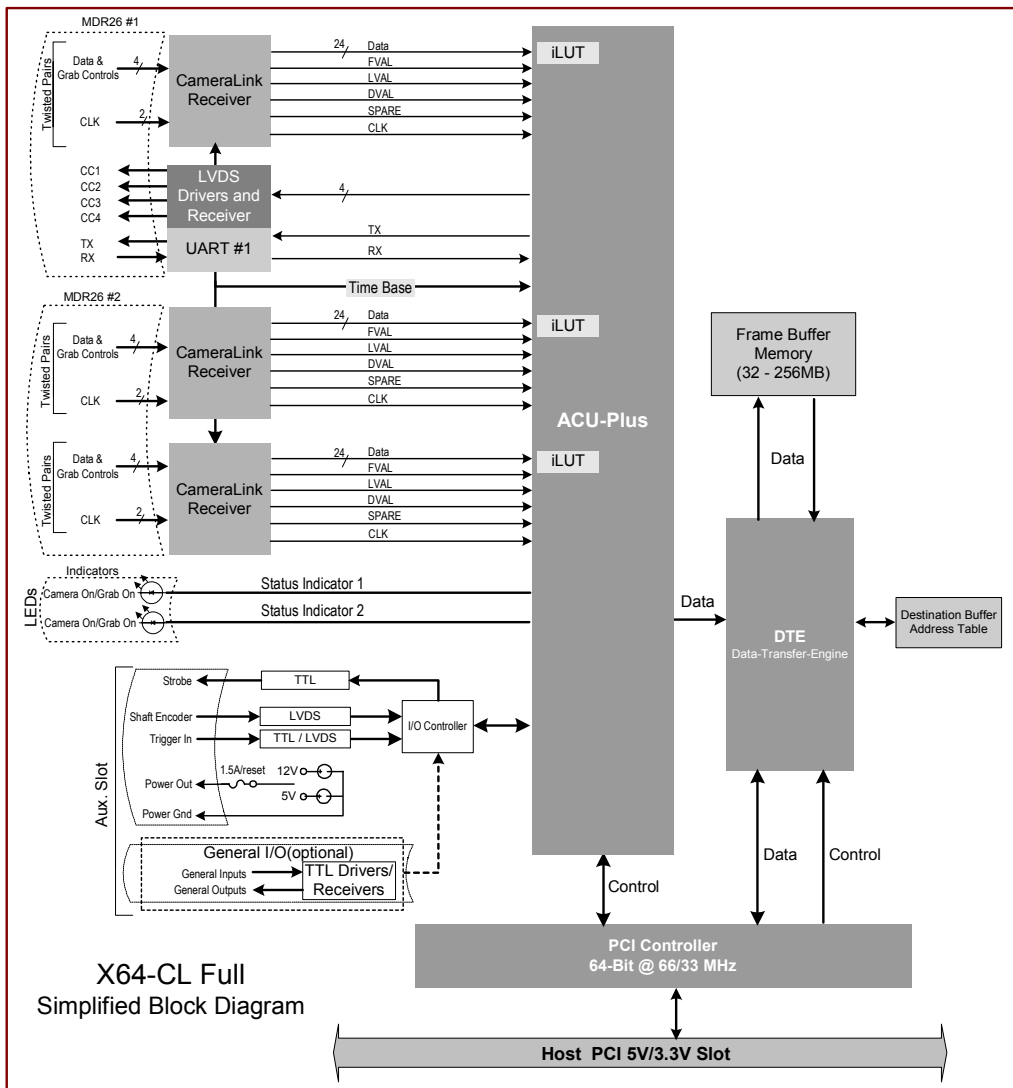
- **Buffer:** Select from supported frame buffer counts, size, and types.



- **Count and Size:** Provides selection of the number of frame buffers and the image size.
- **Type – Contiguous:** Frame buffers are allocated in contiguous system memory (single memory block - no segmentation).
- **Type – Scatter-Gather:** Frame buffers are allocated throughout system memory in noncontiguous memory (paged pool). Pages are locked in physical memory so a scatter-gather list can be constructed. This type allows the allocation of very large size buffers or large buffer count.
- **Type – Off-screen Video:** The buffer is allocated in off-screen video memory and uses the display adapter hardware to perform a fast copy from video memory to video memory.
- **Type – Overlay:** The frame buffer is allocated in video memory where the display adapter overlay hardware uses color-keying to view the overlay buffer.
- **Format:** Shows frame buffer pixel format as supported by the hardware and camera files used.

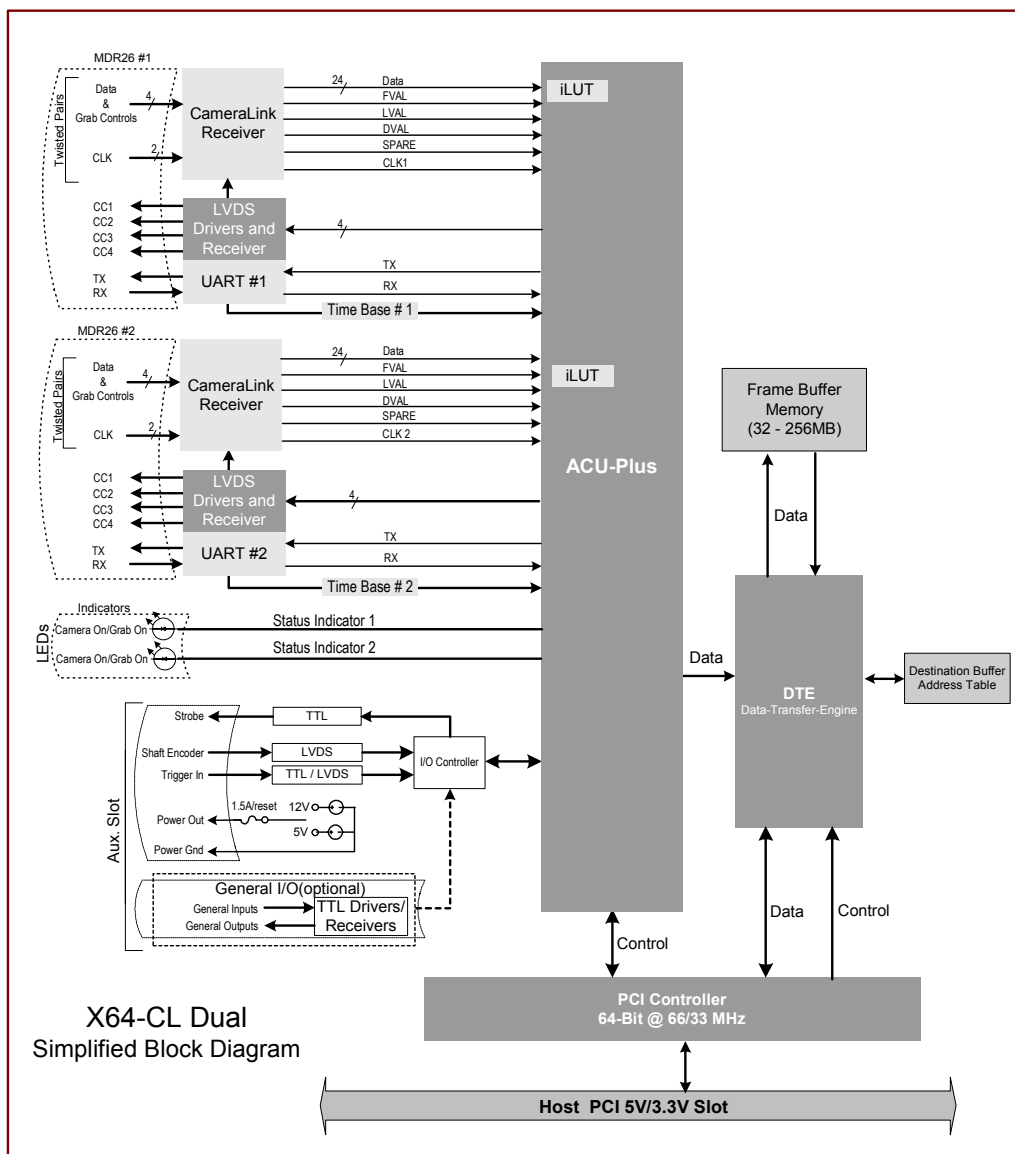
# X64-CL Reference

## X64-CL Full Block Diagram

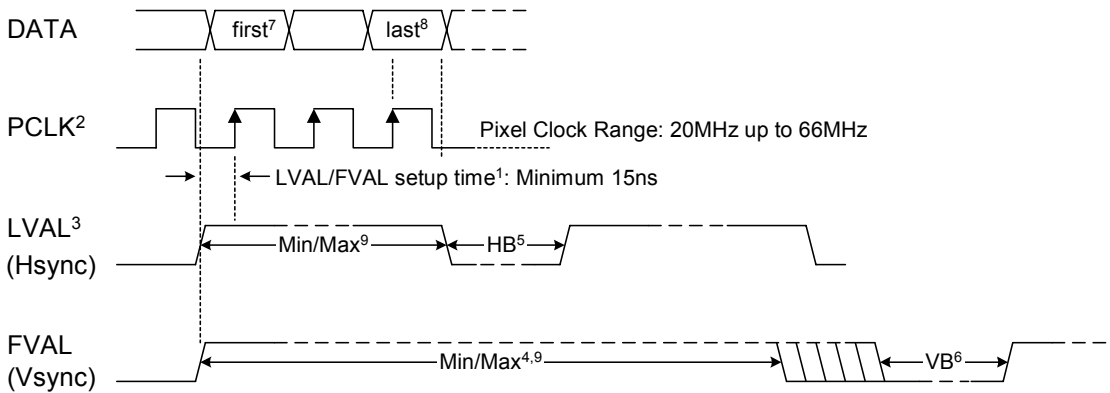


X64-CL Full  
Simplified Block Diagram

# X64-CL Dual Block Diagram



# X64-CL Acquisition Timing



- <sup>1</sup> The setup times for LVAL and FVAL are the same. Both must be high and stable before the rising edge of the Pixel Clock.
- <sup>2</sup> Pixel Clock must always be present.
- <sup>3</sup> LVAL must be active high to acquire camera data.
- <sup>4</sup> Minimum of 1.
- <sup>5</sup> HB - Horizontal Blanking:
  - Minimum: 4 clocks/cycle
  - Maximum: no limits
- <sup>6</sup> VB - Vertical Blanking:
  - Minimum: 1 line
  - Maximum: no limits
- <sup>7</sup> First Active Pixel (unless otherwise specified in the CCA file – "Horizontal Back invalid = x" where 'x' defines the number of pixels to be skipped).
- <sup>8</sup> Last Active Pixel – defined in the CCA file under "Horizontal active = y" – where 'y' is the total number of active pixels per tap.
- <sup>9</sup> Maximum Valid Data:
  - 8-bits/pixel x 256K Pixels/line (LVAL)
  - 16-bits/pixel x 128K Pixels/line (LVAL)
  - 32-bits/pixel x 64K Pixels/line (LVAL)
  - 64-bits/pixel x 32K Pixels/line (LVAL)
  - 16,000,000 lines (FVAL)

---

# Line Trigger Source Selection for Linescan Applications

Linescan imaging applications require some form of external event trigger to synchronize linescan camera exposures to the moving object. This synchronization signal is either an external trigger source (one exposure per trigger event) or a shaft encoder source composed of a single or dual phase (quadrature) signal. The X64-CL shaft encoder inputs provide additional functionality with pulse drop or pulse multiply support.

The following table describes the line trigger source types supported by either the X64-CL Full or X64-CL Dual boards. Refer to the Spera Acquisition Parameters Reference Manual (OC-SAPM-APR00) for descriptions of the Spera parameters.

## CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE – Parameter Values Specific to the X64-CL

PRM Value	Active Shaft Encoder Input
0	Default
1	Use phase A
2	Use phase B
3	Use phase A & B

**CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE full description relative to trigger type and X64-CL model used:**

<b>PRM Value</b>	<b>X64-CL model &amp; camera input used</b>	<b>External Line Trigger Signal used</b>	<b>External Shaft Encoder Signal used</b>
		<i>if</i> CORACQ_PRM_EXT_LINE_TRIGGER_ENABLE = <i>true</i>	<i>if</i> CORACQ_PRM_SHAFT_ENCODER_ENABLE = <i>true</i>
<b>0</b>	Dual - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
	Dual - Camera #2	Shaft Encoder Phase B	Shaft Encoder Phase B
	Full - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A & B
<b>1</b>	Dual - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
	Dual - Camera #2	Shaft Encoder Phase A	Shaft Encoder Phase A
	Full - Camera #1	Shaft Encoder Phase A	Shaft Encoder Phase A
<b>2</b>	Dual - Camera #1	Shaft Encoder Phase B	Shaft Encoder Phase B
	Dual - Camera #2	Shaft Encoder Phase B	Shaft Encoder Phase B
	Full - Camera #1	Shaft Encoder Phase B	Shaft Encoder Phase B
<b>3</b>	Dual - Camera #1	n/a	Shaft Encoder Phase A & B
	Dual - Camera #2	n/a	Shaft Encoder Phase A & B
	Full - Camera #1	n/a	n/a – use prm value = 0

See "J4 (CL) (EM rev. A0, A1): I/O Connector Block" on page 86 for shaft encoder input connector details.

**CVI/CCF File Parameters Used**

- External Line Trigger Source = prm value
- External Line Trigger Enable = true/false
- Shaft Encoder Enable = true/false

---

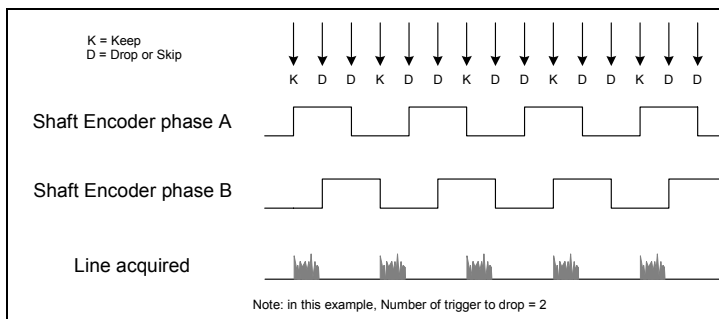
# Shaft Encoder Interface Timing

## Connector J4, Dual Balanced Shaft Encoder Inputs:

- Input 1: Pin 15 (Phase A +) & Pin 16 (Phase A -)  
(see "J4 (CL) (EM rev. A0, A1): I/O Connector Block" on page 86 for complete connector signal details)
- Input 2: Pin 17 (Phase B +) & Pin 18 (Phase B -)
- Use I/O cable assembly OC-64CC-0TIO1  
(see "X64-CL I/O Connector Bracket Assembly" on page 89 for pinout)

Web inspection systems with variable web speeds typically provide one or two synchronization signals from a web mounted encoder to coordinate trigger signals. These trigger signals are used by the acquisition linescan camera. The X64-CL supports single or dual shaft encoder signals. Dual encoder signals are typically 90 degrees out of phase relative to each other and provide greater web motion resolution. When using only one shaft encoder input phase, say phase A, then the phase B inputs must be terminated by connecting the + input to a voltage a minimum of 100 mV positive relative to the – input.

When enabled, the camera is triggered and acquires one scan line for each shaft encoder pulse edge. To optimize the web application, a second Sapera parameter defines the number of triggers to skip between valid acquisition triggers. The figure below depicts a system where a valid camera trigger is any pulse edge from either shaft encoder signal. After a trigger the two following triggers are ignored (as defined by a Sapera parameter).



---

Note that camera file parameters are best modified by using the Sapera CamExpert program.

---

## CVI/CCF File Parameters Used

**Shaft Encoder Enable** = X, where:

- If X = 1, Shaft Encoder is enabled
- If X = 0, Shaft Encoder is disabled

**Shaft Encoder Pulse Drop** = X, where:

- X = number of trigger pulses ignored between valid triggers

---

## Virtual Frame\_Reset for Linescan Cameras

When using linescan cameras a frame buffer is allocated in host system memory to store captured video lines. To control when a video line is stored as the first line in this “virtual” frame buffer, an external frame trigger signal called **FRAME\_RESET** is used. The number of lines sequentially grabbed and stored in the virtual frame buffer is controlled by the Sopera vertical cropping parameter.

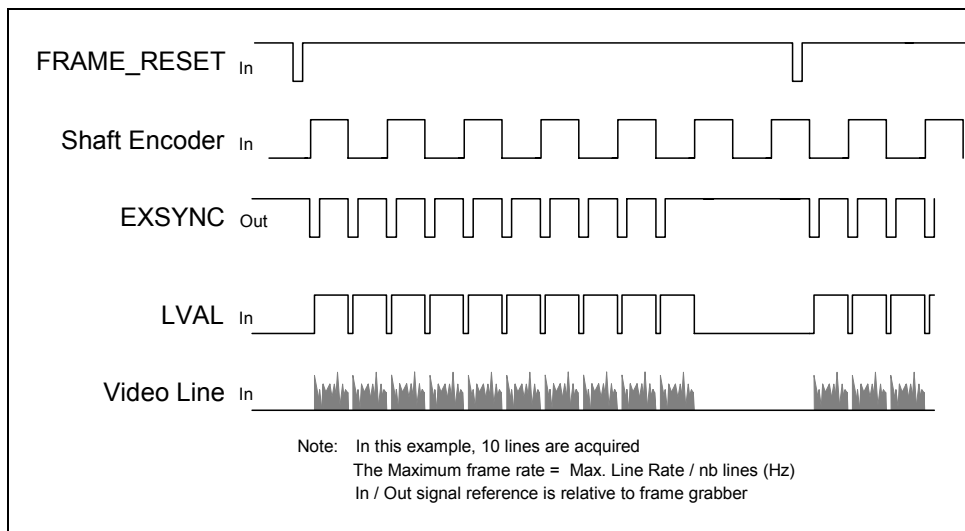
### Virtual Frame\_Reset Timing Diagram

The following timing diagram shows an example of grabbing 10 video lines from a linescan camera and the use of **FRAME\_RESET** to define when a video line is stored at the beginning of the virtual frame buffer. The **FRAME\_RESET** signal (generated by some external event) is input on the X64-CL trigger input.

- **FRAME\_RESET** can be TTL or LVDS and be rising or falling edge active.
- **FRAME\_RESET** control is configured for rising edge trigger in this example.
- **FRAME\_RESET** connects to the X64-CL via the Trigger In 1 balanced inputs on connector J4 pin 11 (+) and 12 (-).
- After the X64-CL receives **FRAME\_RESET**, the **EXSYNC** control signal is output to the camera to trigger n lines of video as per the defined virtual frame size.
- The **EXSYNC** control signal is either based on timing controls input on one or both X64-CL shaft encoder inputs (see “J4 (CL) (EM rev. A0, A1): I/O Connector Block” on page 86 pinout) or an internal X64-CL clock.
- The number of lines captured is specified by the Sopera vertical cropping parameter.

## Synchronization Signals for a Virtual Frame of 10 Lines.

The following timing diagram shows the relationship between external Frame\_Reset input, external Shaft Encoder input (one phase used with the second terminated), and EXSYNC out to the camera.



## CVI File (VIC) Parameters Used

The VIC parameters listed below provide the control functionality for virtual frame reset. Applications either load pre-configured .cvi files or change VIC parameters directly during runtime.

---

Note that camera file parameters are best modified by using the Sopera CamExpert program.

---

**External Frame Trigger Enable** = X, where:                      \\Virtual Frame\_Reset enabled

- If X = 1, External Frame Trigger is enabled
- If X = 0, External Frame Trigger is disabled

**External Frame Trigger Detection** = Y, where:                      \\ Frame\_Reset edge select

- If Y = 4, External Frame Trigger is active on rising edge
- If Y = 8, External Frame Trigger is active on falling edge

**External Frame Trigger Level** = Z, where:                      \\ Frame\_Reset signal type

- If Z = 2, External Frame Trigger is a RS-422/LVDS signal

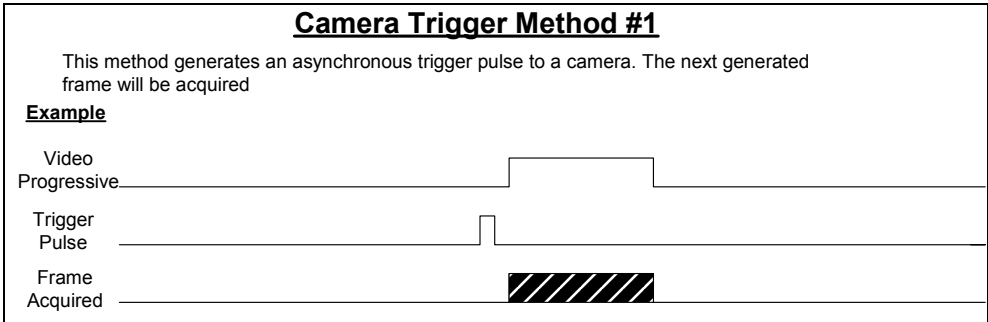
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For information on camera files see the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

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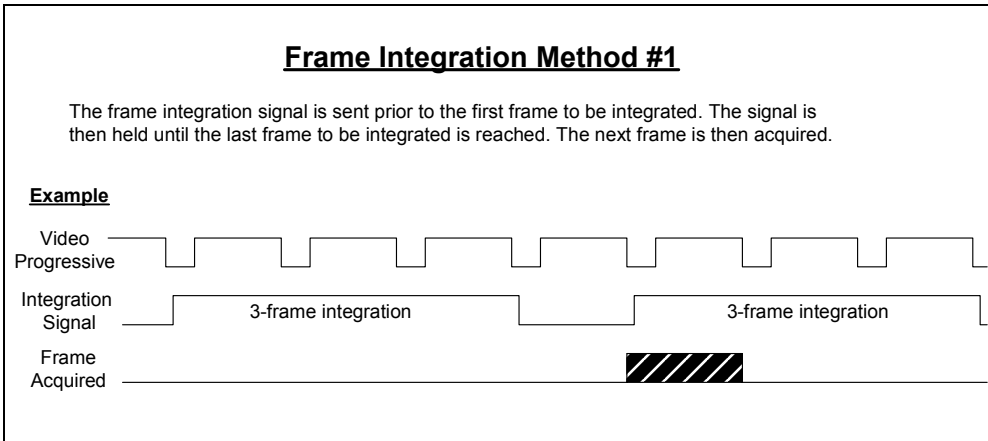
# Acquisition Methods

## Camera Trigger Method #1



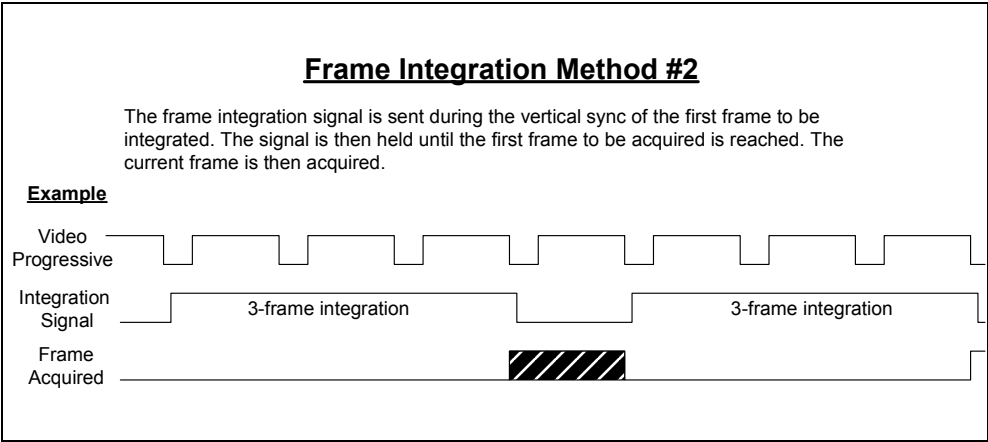
Refer to **CORACQ\_VAL\_CAM\_TRIGGER\_METHOD\_1** in the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

## Frame Integration Method #1



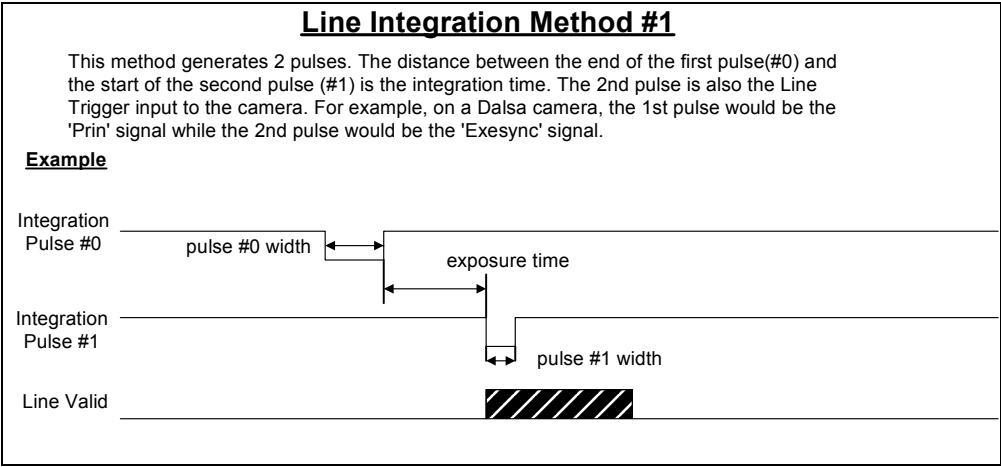
Refer to **CORACQ\_VAL\_FRAME\_INTEGRATE\_METHOD\_1** in the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Frame Integration Method #2



Refer to **CORACQ\_VAL\_FRAME\_INTEGRATE\_METHOD\_2** in the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Line Integration Method #1



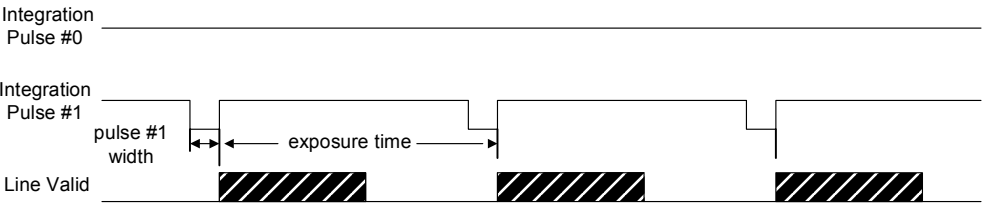
Refer to **CORACQ\_VAL\_LINE\_INTEGRATE\_METHOD\_1** in the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Line Integration Method #2

## Line Integration Method #2

This method generates two consecutive trigger pulses (#1) on the Line Trigger input of the camera. The time interval between the end of the two trigger pulses represents the integration time. An optional signal (#0) with a fixed level might be present. For example, on a Dalsa camera, the Line Trigger input would be the 'Exesync' signal and the optional signal would be the 'Prin' signal.

### Example



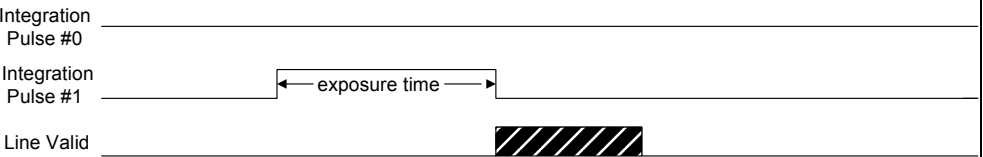
Refer to **CORACQ\_VAL\_LINE\_INTEGRATE\_METHOD\_2** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Line Integration Method #3

## Line Integration Method #3

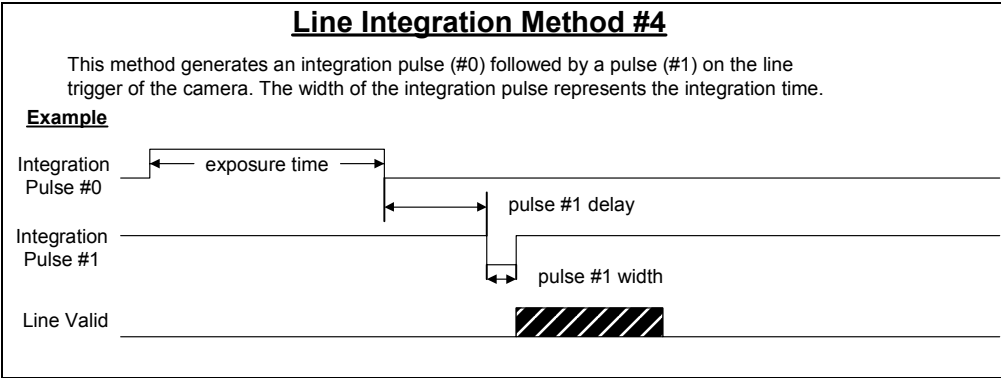
This method generates an asynchronous line integration pulse(#1) to a camera. The width of this pulse represents the integration time. An optional signal (#0) with a fixed level might be present. For example, on a Dalsa camera, the integration pulse would be the 'Exesync' signal and the optional signal would be the 'Prin' signal.

### Example



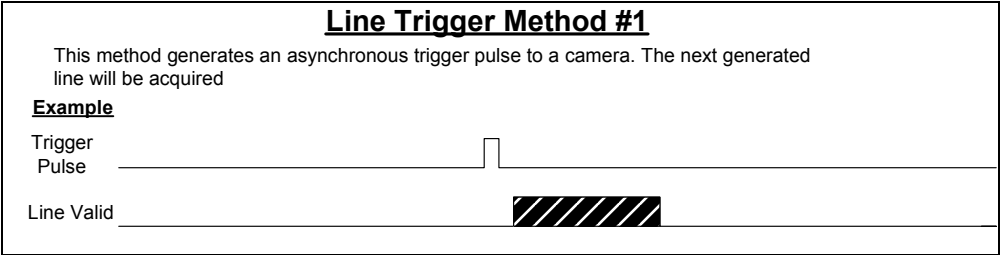
Refer to **CORACQ\_VAL\_LINE\_INTEGRATE\_METHOD\_3** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Line Integration Method #4



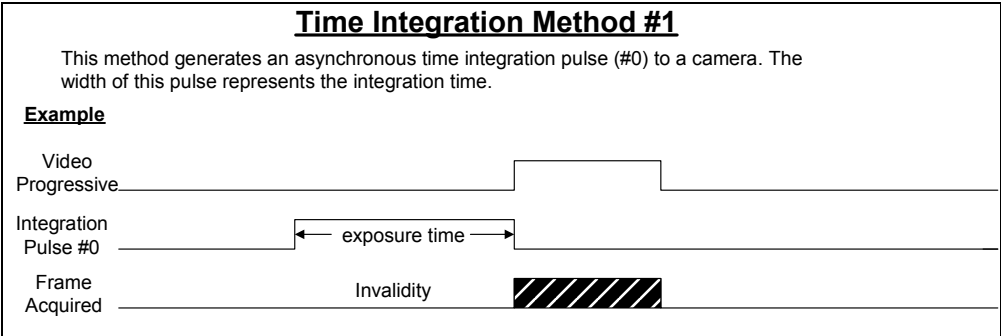
Refer to **CORACQ\_VAL\_LINE\_INTEGRATE\_METHOD\_4** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Line Trigger Method #1



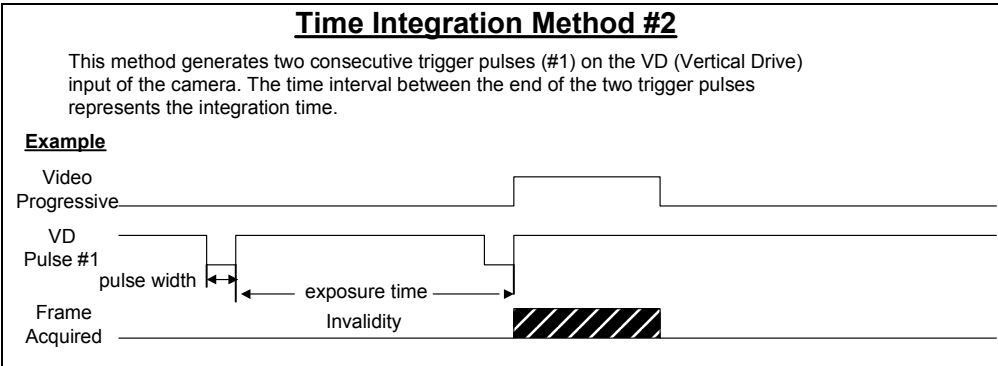
Refer to **CORACQ\_VAL\_LINE\_TRIGGER\_METHOD\_1** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Time Integration Method #1



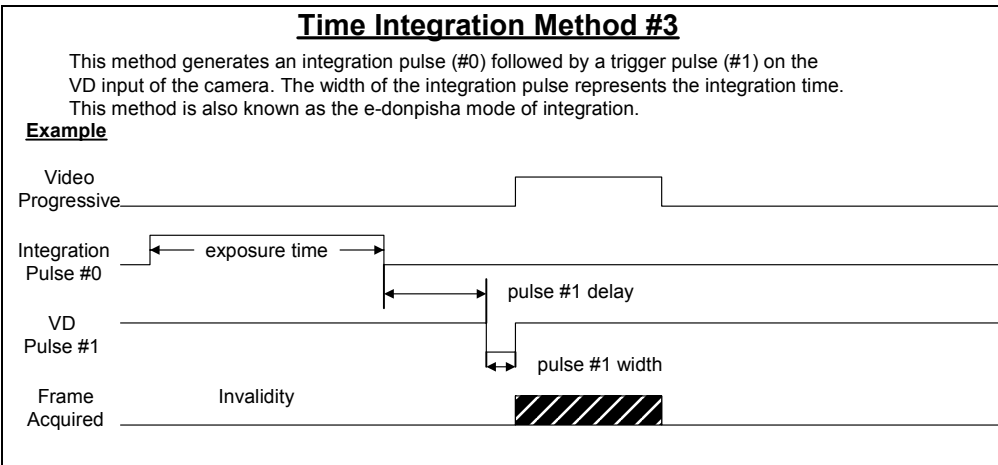
Refer to **CORACQ\_VAL\_TIME\_INTEGRATE\_METHOD\_1** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

## Time Integration Method #2



Refer to **CORACQ\_VAL\_TIME\_INTEGRATE\_METHOD\_2** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

## Time Integration Method #3



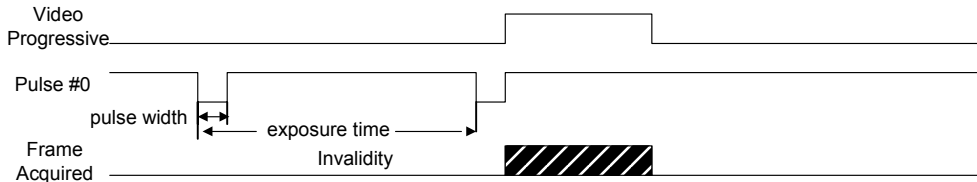
Refer to **CORACQ\_VAL\_TIME\_INTEGRATE\_METHOD\_3** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

## Time Integration Method #4

## Time Integration Method #4

This method generates two consecutive trigger pulses (#0) on the trigger input of the camera. The time interval between the start of the two trigger pulses represents the integration time.

### Example



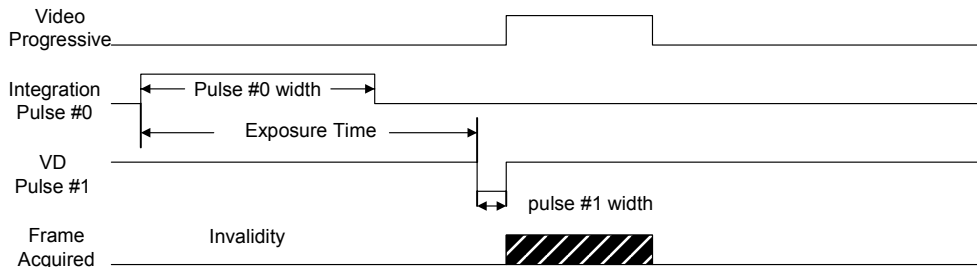
Refer to **CORACQ\_VAL\_TIME\_INTEGRATE\_METHOD\_4** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

## Time Integration Method #5

## Time Integration Method #5

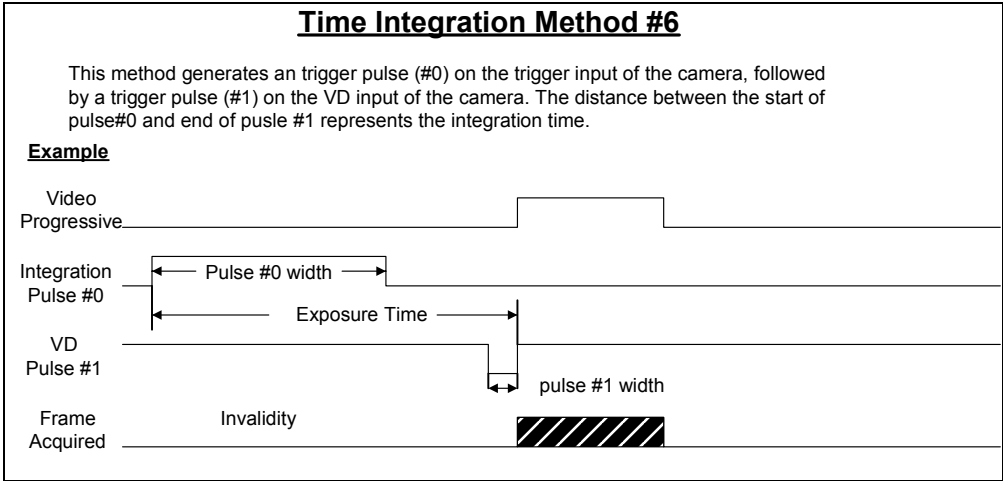
This method generates a trigger pulse (#0) on the trigger input of the camera, followed by a trigger pulse (#1) on the VD input of the camera. The distance between the start of the 2 pulses represents the integration time.

### Example



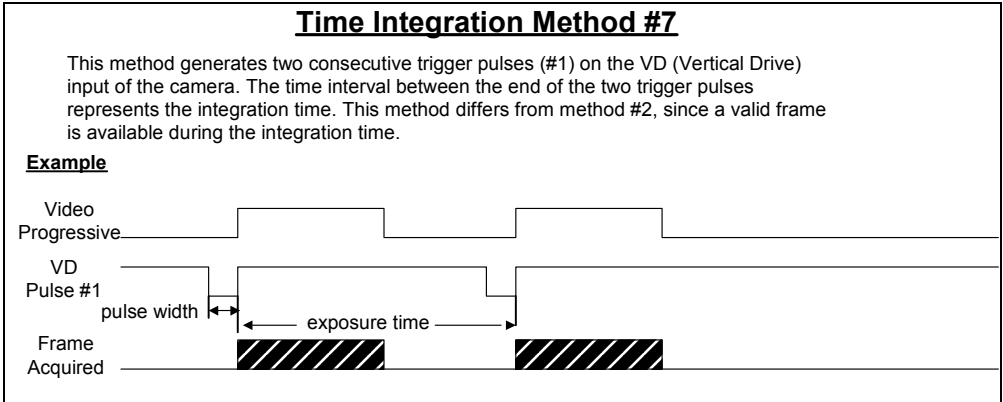
Refer to **CORACQ\_VAL\_TIME\_INTEGRATE\_METHOD\_5** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Time Integration Method #6



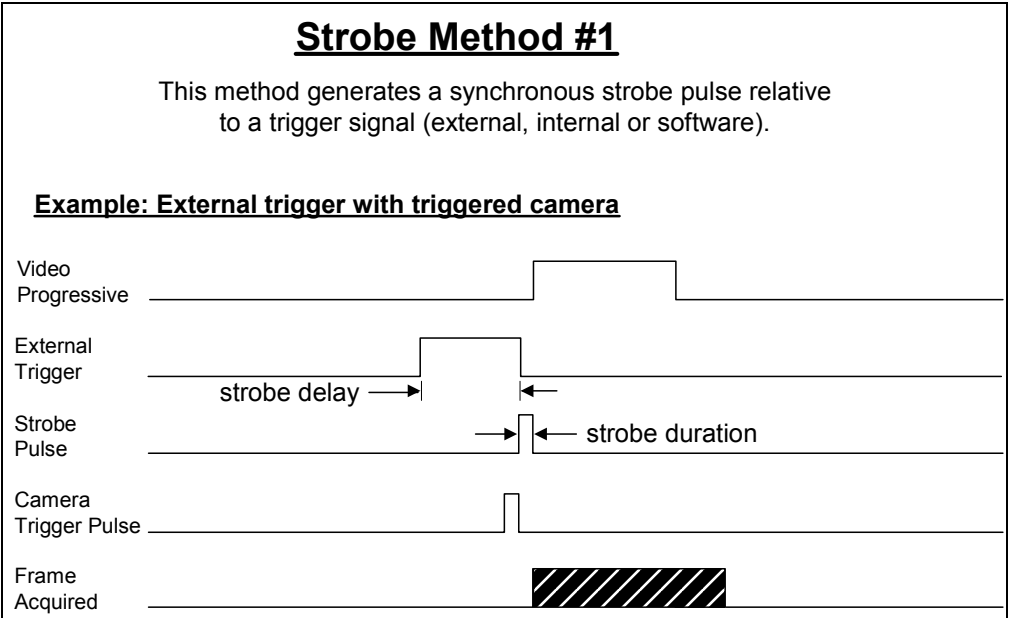
Refer to **CORACQ\_VAL\_TIME\_INTEGRATE\_METHOD\_6** in the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Time Integration Method #7



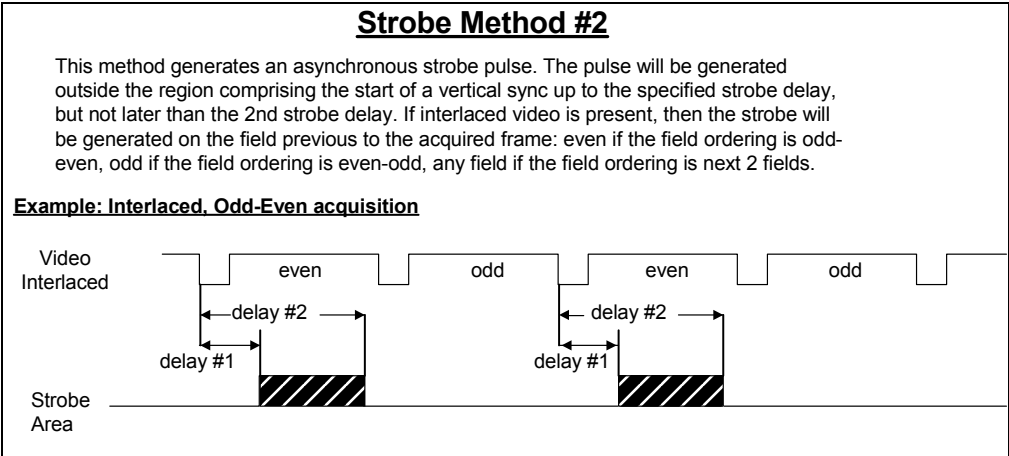
Refer to **CORACQ\_VAL\_TIME\_INTEGRATE\_METHOD\_7** in the Sopera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Strobe Method #1



Refer to **CORACQ\_VAL\_STROBE\_METHOD\_1** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

# Strobe Method #2



Refer to **CORACQ\_VAL\_STROBE\_METHOD\_2** in the Sapera Acquisition Parameters Reference Manual (OC-SAPM-APR00).

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# X64-CL LUT availability

The following tables define the X64-CL input LUT availability and function modes, for the default firmware and optional 12-bit data with LUT firmware.

## Firmware: Standard (default)

Number of Digital Bits	Number of Taps with LUT	Number of Taps Without LUT	Output Pixel Format	LUT Format	Notes
8	1, 2, 4	1, 2, 4, 8	Mono 8	8-in, 8-out	
8	1, 2, 4	1, 2, 4	Mono 16	8-in, 8-out	8 bits in 8 LSBs of 16-bit
10	1, 2, 4	1, 2, 4	Mono 8	10-in, 8-out	LUT is used to convert 10 --> 8
10	1, 2, 4	1, 2, 4	Mono 16	10-in, 10-out	10 bits in 10 LSBs of 16-bit
12	-	-	<i>Mono 8</i>	-	<i>Not supported with standard FPGA</i>
12	0	1, 2, 4	Mono 16	X	
14	-	-	<i>Mono 8</i>	-	<i>Not supported with standard FPGA</i>
14	0	1, 2, 4	Mono 16		
16	-	-	<i>Mono 8</i>	-	<i>Not supported with standard FPGA</i>
16	0	1, 2, 4	Mono 16	X	
8 x 3 (RGB)	1	2	RGB8888	8-in, 8-out	
8 x 3 (RGB)	-	-	<i>RGB101010</i>	-	<i>Not Supported</i>
10 x 3 (RGB)	1	1	RGB8888	10-in, 8-out	LUT is used to convert 10-->8
10 x 3 (RGB)	1	1	RGB101010	10-in, 10-out	

### Notes:

- There is only 1 LUT per camera.
- Since the X64-CL firmware does not keep the MSB data when reducing the number of bits per pixel (i.e. 10 bits -> 8 bits), the LUT is bypassed by loading a ‘normal’ LUT pattern.
- Pixel data bit reduction is only available when the LUT is available.
- X = No LUT available.

## Firmware: X64-CL-DUAL 12-bit LUT

Number of Digital Bits	Number of Taps with LUT	Output Pixel Format	LUT Format	Notes
8	-	MONO 8	-	Not Supported
8	-	MONO 16	-	Not Supported
10	-	MONO 8	-	Not Supported
10	-	MONO 16	-	Not Supported
12	-	MONO 8	-	Not Supported
12	2	MONO 16	12-in, 12-out	12 bits in 12 LSBs of 16-bit
14	-	MONO 8	-	Not Supported
14	-	MONO 16	-	Not Supported
16	-	MONO 8	-	Not Supported
16	-	MONO 16	-	Not Supported
8 x 3 (RGB)	-	RGB8888	-	Not Supported
8 x 3 (RGB)	-	RGB101010	-	Not Supported
10 x 3 (RGB)	-	RGB888	-	Not Supported
10 x 3 (RGB)	-	RGB101010	-	Not Supported
12 x 3 (RGB)	1	RGB161616	12-in, 12-out	12 bits in 12 LSBs of (16-bit x 3)

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# Supporting Non-Standard CameraLink Cameras

Hi performance cameras that output 10 taps can not be interfaced with a standard CameraLink full specification frame grabber. The X64-CL (85 MHz version) provides support for non-standard 10-tap formats by using specific firmware versions that are easily uploaded when required. Two formats are described below along with an example camera for each non-standard format.

## Firmware: X64-CL 10-Tap Format 1

- Requires X64-CL 85 MHz board
- X64-CL 10 Taps Format 1 firmware supports cameras such as Vosskuhler CMC-1300.
- This CameraLink utilization is not compatible with the standard 8 tap full specification.
- No LUT available on the X64-CL.
- The following table describes the Bit assignment of Format 1.
- Tap 1 Bits are D0\_x ... Tap 10 Bits are D9\_x

Connector 1 Channel Link No. X		Connector 2 Channel Link No. Y		Connector 2 Channel Link No. Z	
Bit Name	Input/Output Pin	Bit Name	Input/Output Pin	Bit Name	Input/Output Pin
D0_0	Tx0/Rx0	D3_0	Tx0/Rx0	D6_0	Tx0/Rx0
D0_1	Tx1/Rx1	D3_1	Tx1/Rx1	D6_1	Tx1/Rx1
D0_2	Tx2/Rx2	D3_2	Tx2/Rx2	D6_2	Tx2/Rx2
D0_3	Tx3/Rx3	D3_3	Tx3/Rx3	D6_3	Tx3/Rx3
D0_4	Tx4/Rx4	D3_4	Tx4/Rx4	D6_4	Tx4/Rx4
D0_5	Tx6/Rx6	D3_5	Tx6/Rx6	D6_5	Tx6/Rx6
D0_6	Tx27/Rx27	D3_6	Tx27/Rx27	D6_6	Tx27/Rx27
D0_7	Tx5/Rx5	D3_7	Tx5/Rx5	D6_7	Tx5/Rx5
D1_0	Tx7/Rx7	D4_0	Tx7/Rx7	D7_0	Tx7/Rx7
D1_1	Tx8/Rx8	D4_1	Tx8/Rx8	D7_1	Tx8/Rx8
D1_2	Tx9/Rx9	D4_2	Tx9/Rx9	D7_2	Tx9/Rx9
D1_3	Tx12/Rx12	D4_3	Tx12/Rx12	D7_3	Tx12/Rx12
D1_4	Tx13/Rx13	D4_4	Tx13/Rx13	D7_4	Tx13/Rx13
D1_5	Tx14/Rx14	D4_5	Tx14/Rx14	D7_5	Tx14/Rx14
D1_6	Tx10/Rx10	D4_6	Tx10/Rx10	D7_6	Tx10/Rx10

D1_7	Tx10/Rx11	D4_7	Tx10/Rx11	D7_7	Tx10/Rx11
D2_0	Tx15/Rx15	D5_0	Tx15/Rx15	D8_0	Tx15/Rx15
D2_1	Tx18/Rx18	D5_1	Tx18/Rx18	D8_1	Tx18/Rx18
D2_2	Tx19/Rx19	D5_2	Tx19/Rx19	D8_2	Tx19/Rx19
D2_3	Tx20/Rx20	D5_3	Tx20/Rx20	D8_3	Tx20/Rx20
D2_4	Tx21/Rx21	D5_4	Tx21/Rx21	D8_4	Tx21/Rx21
D2_5	Tx22/Rx22	D5_5	Tx22/Rx22	D8_5	Tx22/Rx22
D2_6	Tx16/Rx16	D5_6	Tx16/Rx16	D8_6	Tx16/Rx16
D2_7	Tx17/Rx17	D5_7	Tx17/Rx17	D8_7	Tx17/Rx17
LVAL	Tx24/Rx24	D9_1	Tx24/Rx24	D9_5	Tx24/Rx24
FVAL	Tx25/Rx25	D9_2	Tx25/Rx25	D9_6	Tx25/Rx25
DVAL	Tx26/Rx26	D9_3	Tx26/Rx26	D9_7	Tx26/Rx26
Spare	Tx23/Rx23	D9_0	Tx23/Rx23	D9_4	Tx23/Rx23

## Firmware: X64-CL 10-Tap Format 2

- Requires X64-CL 85 MHz board
- Supports 10-tap Format 2 cameras only such as Basler A504K
- This CameraLink utilization is not compatible with the standard 8 tap full specification.
- No LUT available on the X64-CL.
- The following table describes the Bit assignment of Format 2.
- Tap 1 Bits are D0\_x ... Tap 10 Bits are D9\_x

Connector 1 Channel Link No. X		Connector 2 Channel Link No. Y		Connector 2 Channel Link No. Z	
Bit Name	Input/Output Pin	Bit Name	Input/Output Pin	Bit Name	Input/Output Pin
D0_0	Tx0/Rx0	D3_2	Tx0/Rx0	D6_5	Tx0/Rx0
D0_1	Tx1/Rx1	D3_3	Tx1/Rx1	D6_6	Tx1/Rx1
D0_2	Tx2/Rx2	D3_4	Tx2/Rx2	D6_7	Tx2/Rx2
D0_3	Tx3/Rx3	D3_5	Tx3/Rx3	D7_0	Tx3/Rx3
D0_4	Tx4/Rx4	D3_6	Tx4/Rx4	D7_1	Tx4/Rx4
D0_5	Tx5/Rx5	D3_7	Tx5/Rx5	D7_2	Tx5/Rx5

D0_6	Tx6/Rx6	D4_0	Tx6/Rx6	D7_3	Tx6/Rx6
D0_7	Tx7/Rx7	D4_1	Tx7/Rx7	D7_4	Tx7/Rx7
D1_0	Tx8/Rx8	D4_2	Tx8/Rx8	D7_5	Tx8/Rx8
D1_1	Tx9/Rx9	D4_3	Tx9/Rx9	D7_6	Tx9/Rx9
D1_2	Tx10/Rx10	D4_4	Tx10/Rx10	D7_7	Tx10/Rx10
D1_3	Tx11/Rx11	D4_5	Tx11/Rx11	D8_0	Tx11/Rx11
D1_4	Tx12/Rx12	D4_6	Tx12/Rx12	D8_1	Tx12/Rx12
D1_5	Tx13/Rx13	D4_7	Tx13/Rx13	D8_2	Tx13/Rx13
D1_6	Tx14/Rx14	D5_0	Tx14/Rx14	D8_3	Tx14/Rx14
D1_7	Tx15/Rx15	D5_1	Tx15/Rx15	D8_4	Tx15/Rx15
D2_0	Tx16/Rx16	D5_2	Tx16/Rx16	D8_5	Tx16/Rx16
D2_1	Tx17/Rx17	D5_3	Tx17/Rx17	D8_6	Tx17/Rx17
D2_2	Tx18/Rx18	D5_4	Tx18/Rx18	D8_7	Tx18/Rx18
D2_3	Tx19/Rx19	D5_5	Tx19/Rx19	D9_0	Tx19/Rx19
D2_4	Tx20/Rx20	D5_6	Tx20/Rx20	D9_1	Tx20/Rx20
D2_5	Tx21/Rx21	D5_7	Tx21/Rx21	D9_2	Tx21/Rx21
D2_6	Tx22/Rx22	D6_0	Tx22/Rx22	D9_3	Tx22/Rx22
D2_7	Tx23/Rx23	D6_1	Tx23/Rx23	D9_4	Tx23/Rx23
LVAL	Tx24/Rx24	D6_2	Tx24/Rx24	D9_5	Tx24/Rx24
FVAL	Tx25/Rx25	D6_3	Tx25/Rx25	D9_6	Tx25/Rx25
D3_0	Tx26/Rx26	D6_4	Tx26/Rx26	D9_7	Tx26/Rx26
D3_1	Tx27/Rx27	LVAL	Tx27/Rx27	LVAL	Tx27/Rx27

# X64-CL Sopera Capabilities

The three tables below describe the Sopera capabilities supported by the X64-CL Full and X64-CL Dual boards. Unless specified, each capability applies to both boards and all acquisition modes. Other Sopera capabilities have been omitted for clarity.

Specifically the X64-CL family is described in Sopera as:

- Board Server: X64\_1
- Acquisition Device: CameraLink
- Acquisition Modes (X64-CL Full): Full Mono or Medium Color RGB
- Acquisition Modes (X64-CL Dual): Base Mono or Base Color RGB

## Camera Related Capabilities

Capability	Value or Limits or Bitfield	Capability Description / Details
CORACQ_CAP_CAMLINK_CONFIGURATION (Base Color RGB)	00000001b	(0x1) Base configuration
CORACQ_CAP_CAMLINK_CONFIGURATION (Base Mono)	00000001b	(0x1) Base configuration
CORACQ_CAP_CAMLINK_CONFIGURATION (Full Mono)	00000111b	(0x1) Base configuration (0x2) Medium configuration (0x4) Full configuration
CORACQ_CAP_CAMLINK_CONFIGURATION (Medium Color RGB)	00000011b	(0x1) Base configuration (0x2) Medium configuration
CORACQ_CAP_CHANNEL	1	(0x1) CORACQ_VAL_CHANNEL_SINGLE
CORACQ_CAP_CHANNELS_ORDER	00000011b	(0x1) CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x2) CORACQ_VAL_CHANNELS_ORDER_REVERSE
CORACQ_CAP_DATA_VALID_ENABLE	1	(0x1) True The camera data valid signal is supported
CORACQ_CAP_DATA_VALID_POLARITY	00000010b	(0x2) Data valid signal active high
CORACQ_CAP_FIELD_ORDER	00000100b	(0x4) CORACQ_VAL_FIELD_ORDER_NEXT_FIELD
CORACQ_CAP_FRAME	00000010b	(0x2) CORACQ_VAL_FRAME_PROGRESSIVE
CORACQ_CAP_HACTIVE_MAX	16777215	(0xffffffff) maximum pixels per tap
CORACQ_CAP_HACTIVE_MIN	1	(0x01) minimum pixel per tap
CORACQ_CAP_HACTIVE_MULT	1	0x1
CORACQ_CAP_HBACK_INVALID_MAX	16777215	0xffffffff
CORACQ_CAP_HBACK_INVALID_MIN	0	0x0
CORACQ_CAP_HBACK_INVALID_MULT	1	0x1
CORACQ_CAP_HFRONT_INVALID_MAX	16777215	0xffffffff
CORACQ_CAP_HFRONT_INVALID_MIN	0	0x0
CORACQ_CAP_HFRONT_INVALID_MULT	1	0x1
CORACQ_CAP_HSYNC_MAX	4294967295	0xffffffff

CORACQ_CAP_HSYNC_MIN	1	(0x1) minimum pixel per tap
CORACQ_CAP_HSYNC_MULT	1	0x1
CORACQ_CAP_HSYNC_POLARITY	1	(0x1) Horizontal sync pulse is active low
CORACQ_CAP_INTERFACE	00000010b	(0x2) CORACQ_VAL_INTERFACE_DIGITAL
CORACQ_CAP_LINE_INTEGRATE	1	(0x1) True At least one method of line integration is supported
CORACQ_CAP_LINE_INTEGRATE_METHOD	00001111b	(0x01) Line Integration Method #1 (0x02) Line Integration Method #2 (0x04) Line Integration Method #3 (0x08) Line Integration Method #4
CORACQ_CAP_LINE_INTEGRATE_PULSE0_DELAY_MAX	65535	0xffff (in pixels)
CORACQ_CAP_LINE_INTEGRATE_PULSE0_DELAY_MIN	0	0x0
CORACQ_CAP_LINE_INTEGRATE_PULSE0_DURATION_MAX	65535000	0x3e7fc18 (in pixels)
CORACQ_CAP_LINE_INTEGRATE_PULSE0_DURATION_MIN	1	0x1
CORACQ_CAP_LINE_INTEGRATE_PULSE0_POLARITY	00000011b	(0x1) Line integration trigger pulse is active low (0x2) Line integration trigger pulse is active high.
CORACQ_CAP_LINE_INTEGRATE_PULSE1_DELAY_MAX	65535000	0x3e7fc18 (in pixels)
CORACQ_CAP_LINE_INTEGRATE_PULSE1_DELAY_MIN	0	0x0
CORACQ_CAP_LINE_INTEGRATE_PULSE1_DURATION_MAX	65535000	0x3e7fc18 (in pixels)
CORACQ_CAP_LINE_INTEGRATE_PULSE1_DURATION_MIN	1	0x1
CORACQ_CAP_LINE_INTEGRATE_PULSE1_POLARITY	00000011b	(0x1) Line integration trigger pulse is active low (0x2) Line integration trigger pulse is active high.
CORACQ_CAP_LINE_TRIGGER	1	(0x1) True At least one method of line trigger is supported
CORACQ_CAP_LINE_TRIGGER_DELAY_MAX	65535	(0xffff)
CORACQ_CAP_LINE_TRIGGER_DELAY_MIN	0	(0x0)
CORACQ_CAP_LINE_TRIGGER_DURATION_MAX	65535	(0xffff)
CORACQ_CAP_LINE_TRIGGER_DURATION_MIN	0	(0x0)
CORACQ_CAP_LINE_TRIGGER_METHOD	1	(0x1) Line Trigger Method #1
CORACQ_CAP_LINE_TRIGGER_POLARITY	00000011b	(0x01) CORACQ_VAL_ACTIVE_LOW (0x02) CORACQ_VAL_ACTIVE_HIGH
CORACQ_CAP_LINESCAN_DIRECTION	1	(0x1) True Line scan direction signal can be controlled by the acquisition device
CORACQ_CAP_LINESCAN_DIRECTION_POLARITY	00000010b	(0x2) Forward direction scan signal is active high
CORACQ_CAP_PIXEL_CLK_DETECTION	00000100b	(0x4) CORACQ_VAL_RISING_EDGE
CORACQ_CAP_PIXEL_CLK_EXT_MAX	66000000	0x3ef1480
CORACQ_CAP_PIXEL_CLK_EXT_MIN	20000000	0x1312d00
CORACQ_CAP_PIXEL_CLK_SRC	00000010b	(0x2) External pixel clock

CORACQ_CAP_PIXEL_DEPTH		8 bit	1 LUT where format = 0x1010800, (see Sapera Basic: LUT File Format)
CORACQ_CAP_PIXEL_DEPTH		10 bit	1 LUT where format = 0x1000A00, (see Sapera Basic: LUT File Format)
CORACQ_CAP_PIXEL_DEPTH		12	no LUT
CORACQ_CAP_PIXEL_DEPTH		14	no LUT
CORACQ_CAP_PIXEL_DEPTH		16	no LUT
CORACQ_CAP_PIXEL_DEPTH		32	no LUT
CORACQ_CAP_PIXEL_DEPTH_PER_TAP		8	(0x8)
CORACQ_CAP_SCAN		00000011b	(0x1) CORACQ_VAL_SCAN_AREA (0x2) CORACQ_VAL_SCAN_LINE
CORACQ_CAP_SIGNAL		00000010b	(0x2) CORACQ_VAL_SIGNAL_DIFFERENTIAL
CORACQ_CAP_SYNC		00000100b	(0x4) Separate horizontal and vertical sync source.
CORACQ_CAP_TAP_DIRECTION		01111111b	(0x01)CORACQ_VAL_TAP_DIRECTION_LR (0x02)CORACQ_VAL_TAP_DIRECTION_RL (0x04)CORACQ_VAL_TAP_DIRECTION_UD (0x08)CORACQ_VAL_TAP_DIRECTION_DU (0x10)CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x20)CORACQ_VAL_TAP_DIRECTION_FROM_MID (0x40)CORACQ_VAL_TAP_DIRECTION_FROM_BOT
CORACQ_CAP_TAP_OUTPUT		00000111b	(0x01) CORACQ_VAL_TAP_OUTPUT_ALTERNATE (0x02) CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x04) CORACQ_VAL_TAP_OUTPUT_PARALLEL
CORACQ_CAP_TAPS	(Base Color RGB)	2	(0x2) max Taps
CORACQ_CAP_TAPS	(Base Mono)	3	(0x3) max Taps
CORACQ_CAP_TAPS	(Full Mono)	10	(0xa) max Taps
CORACQ_CAP_TAPS	(Medium Color RGB)	2	(0x2) max Taps
CORACQ_CAP_TIME_INTEGRATE		1	(0x1) True At least one method of time integration is supported
CORACQ_CAP_TIME_INTEGRATE_METHOD		01111111b	(0x01) Time Integration Method #1 (0x02) Time Integration Method #2 (0x04) Time Integration Method #3 (0x08) Time Integration Method #4 (0x10) Time Integration Method #5 (0x20) Time Integration Method #6 (0x40) Time Integration Method #7
CORACQ_CAP_TIME_INTEGRATE_PULSE0_DELAY_MAX		65535000	0x3e7fc18 (in μs)
CORACQ_CAP_TIME_INTEGRATE_PULSE0_DELAY_MIN		0	0x0
CORACQ_CAP_TIME_INTEGRATE_PULSE0_DURATION_MAX		65535000	0x3e7fc18 (in μs)
CORACQ_CAP_TIME_INTEGRATE_PULSE0_DURATION_MIN		1	0x1
CORACQ_CAP_TIME_INTEGRATE_PULSE0_POLARITY		00000011b	(0x1) Time integration trigger pulse is active low (0x2) Time integration trigger pulse is active high.
CORACQ_CAP_TIME_INTEGRATE_PULSE1_DELAY_MAX		65535000	0x3e7fc18 (in μs)
CORACQ_CAP_TIME_INTEGRATE_PULSE1_DELAY_MIN		0	0x0
CORACQ_CAP_TIME_INTEGRATE_PULSE1_DURATION_MAX		65535000	0x3e7fc18 (in μs)

CORACQ_CAP_TIME_INTEGRATE_PULSE1_DURATION_MIN	1	0x1
CORACQ_CAP_TIME_INTEGRATE_PULSE1_POLARITY	00000011b	(0x1) Time integration trigger pulse is active low (0x2) Time integration trigger pulse is active high.
CORACQ_CAP_VACTIVE_MAX	16777215	0xffffffff lines
CORACQ_CAP_VACTIVE_MIN	1	0x1 line
CORACQ_CAP_VACTIVE_MULT	1	0x1
CORACQ_CAP_VBACK_INVALID_MAX	16777215	0xffffffff
CORACQ_CAP_VBACK_INVALID_MIN	0	0x0
CORACQ_CAP_VBACK_INVALID_MULT	1	0x1
CORACQ_CAP_VFRONT_INVALID_MAX	16777215	0xffffffff
CORACQ_CAP_VFRONT_INVALID_MIN	0	0x0
CORACQ_CAP_VFRONT_INVALID_MULT	1	0x1
CORACQ_CAP_VIDEO	<i>(Full / Dual Mono)</i>	00000001b (0x1) CORACQ_VAL_VIDEO_MONO
CORACQ_CAP_VIDEO	<i>(Medium / Base Color RGB)</i>	00001000b (0x8) CORACQ_VAL_VIDEO_RGB
CORACQ_CAP_VIDEO_STD	1	(0x1) CORACQ_VAL_VIDEO_STD_NON_STD
CORACQ_CAP_VSYNC_MAX	4294967295	0xfffffffff
CORACQ_CAP_VSYNC_MIN	0	0x0
CORACQ_CAP_VSYNC_MULT	1	0x1
CORACQ_CAP_VSYNC_POLARITY	1	(0x1) Vertical sync pulse is active low

## VIC Related Capabilities

Capability	Value or Limits or Bitfield	Capability Description / Details
CORACQ_CAP_BIT_ORDERING	1	(0x1) Standard digital bit ordering
CORACQ_CAP_CAMSEL_MONO	1	(0x1) camera supported
CORACQ_CAP_CAMSEL_RGB	1	(0x1) camera supported
CORACQ_CAP_CROP_HEIGHT_MAX	16777215	0xffffffff (in lines)
CORACQ_CAP_CROP_HEIGHT_MIN	1	0x1 (lines)
CORACQ_CAP_CROP_HEIGHT_MULT	1	0x1 (lines)
CORACQ_CAP_CROP_HORZ	1	(0x1) True, horizontal cropping is supported
CORACQ_CAP_CROP_LEFT_MAX	16777215	0xffffffff (in pixels)
CORACQ_CAP_CROP_LEFT_MIN	0	0x0 (in pixels)
CORACQ_CAP_CROP_LEFT_MULT	8	0x8 (pixels)
CORACQ_CAP_CROP_TOP_MAX	16777215	0xffffffff (in lines)
CORACQ_CAP_CROP_TOP_MIN	0	0x0 (in lines)
CORACQ_CAP_CROP_TOP_MULT	1	0x1 (lines)
CORACQ_CAP_CROP_VERT	1	(0x1) True, vertical cropping is supported

CORACQ_CAP_CROP_WIDTH_MAX	16777215	0xffffffff (in pixels)
CORACQ_CAP_CROP_WIDTH_MIN	8	0x8 (pixels)
CORACQ_CAP_CROP_WIDTH_MULT	8	0x8 (pixels)
CORACQ_CAP_DECIMATE_METHOD	00000001b	(0x01) No decimation
CORACQ_CAP_EXT_FRAME_TRIGGER	1	(0x1) True, external frame trigger is available
CORACQ_CAP_EXT_FRAME_TRIGGER_DETECTION	00001111b	(0x01) Active low signal (0x02) Active high signal (0x04) Rising signal edge (0x08) Falling signal edge
CORACQ_CAP_EXT_FRAME_TRIGGER_LEVEL	00000011b	(0x01), A TTL signal level (0x02), A RS-422 signal level
CORACQ_CAP_EXT_LINE_TRIGGER	1	(0x1) True, external line trigger is available
CORACQ_CAP_EXT_LINE_TRIGGER_DETECTION	00001000b	(0x08), Falling signal edge
CORACQ_CAP_EXT_LINE_TRIGGER_LEVEL	00000011b	(0x01), A TTL signal level (0x02), A RS-422 signal level
CORACQ_CAP_EXT_TRIGGER	1	(0x1) True, external trigger is available
CORACQ_CAP_EXT_TRIGGER_DETECTION	00001111b	(0x01) An active low signal. (0x02) An active high signal. (0x04) The rising edge of the signal. (0x08) The falling edge of the signal.
CORACQ_CAP_EXT_TRIGGER_FRAME_COUNT	1	(0x1) True, more than 1 frame can be acquired
CORACQ_CAP_EXT_TRIGGER_LEVEL	00000011b	(0x01), A TTL signal level (0x02), A RS-422 signal level
CORACQ_CAP_EXT_TRIGGER_SOURCE	4	(0x4)
CORACQ_CAP_FRAME_LENGTH	1	(0x1) Fixed length images
CORACQ_CAP_HSYNC_REF	2	(0x2) End of horizontal sync
CORACQ_CAP_INT_FRAME_TRIGGER	1	(0x1) True, internal frame trigger is available
CORACQ_CAP_INT_FRAME_TRIGGER_FREQ_MAX	1073741823	0x3fffffff (in milli-Hz)
CORACQ_CAP_INT_FRAME_TRIGGER_FREQ_MIN	1	0x1 (in milli-Hz)
CORACQ_CAP_INT_LINE_TRIGGER	1	(0x1) True, internal line trigger is available
CORACQ_CAP_LINE_INTEGRATE_DURATION_MAX	16777215	0xffffffff (in pixels)
CORACQ_CAP_LINE_INTEGRATE_DURATION_MIN	1	0x1 (in pixels)
CORACQ_CAP_LUT	1	(0x1) True, at least one LUT is available
CORACQ_CAP_LUT_ENABLE	1	(0x1) True, input LUT can be enabled/disabled
CORACQ_CAP_OUTPUT_FORMAT (Full Mono, Base Mono)		CORACQ_VAL_OUTPUT_FORMAT_MONO8
CORACQ_CAP_OUTPUT_FORMAT (Full Mono, Base Mono)		CORACQ_VAL_OUTPUT_FORMAT_MONO16
CORACQ_CAP_OUTPUT_FORMAT (Medium Color RGB)		CORACQ_VAL_OUTPUT_FORMAT_RGB101010
CORACQ_CAP_OUTPUT_FORMAT (Medium Color RGB, Base Color RGB)		CORACQ_VAL_OUTPUT_FORMAT_RGB8888
CORACQ_CAP_OUTPUT_FORMAT_BYTE_MULT	4	0x4 (in bytes)

CORACQ_CAP_SCALE_HORZ_METHOD	1	(0x1) Disable horizontal scaling
CORACQ_CAP_SCALE_VERT_METHOD	1	(0x1) Disable vertical scaling
CORACQ_CAP_SHAFT_ENCODER	1	(0x1) True, shaft encoder option is available
CORACQ_CAP_SHAFT_ENCODER_DROP	1	(0x1) True, edge dropping is available.
CORACQ_CAP_SHAFT_ENCODER_DROP_MAX	511	(0x1ff)
CORACQ_CAP_SHAFT_ENCODER_DROP_MIN	0	(0x0)
CORACQ_CAP_SHAFT_ENCODER_LEVEL	00000010b	(0x2) a differential signal
CORACQ_CAP_STROBE	1	(0x1) Supports at least one output strobe pulse method
CORACQ_CAP_STROBE_DELAY_2_MAX	65535000	0x3e7fc18(in $\mu$ s)
CORACQ_CAP_STROBE_DELAY_2_MIN	0	0x0 (in $\mu$ s)
CORACQ_CAP_STROBE_DELAY_MAX	65535000	0x3e7fc18(in $\mu$ s)
CORACQ_CAP_STROBE_DELAY_MIN	0	0x0 (in $\mu$ s)
CORACQ_CAP_STROBE_DURATION_MAX	65535000	0x3e7fc18(in $\mu$ s)
CORACQ_CAP_STROBE_DURATION_MIN	0	0x0 (in $\mu$ s)
CORACQ_CAP_STROBE_LEVEL	1	(0x1) A TTL signal.
CORACQ_CAP_STROBE_METHOD	00000011b	(0x01) Strobe Method #1 (0x02) Strobe Method #2
CORACQ_CAP_STROBE_POLARITY	00000011b	(0x1) Strobe pulse will be active low (0x2) Strobe pulse will be active high
CORACQ_CAP_SYNC_CROP_HEIGHT_MAX	16777215	0xffffffff (in lines)
CORACQ_CAP_SYNC_CROP_HEIGHT_MIN	0	0x0 (in lines)
CORACQ_CAP_SYNC_CROP_HEIGHT_MULT	1	0x1 (line)
CORACQ_CAP_SYNC_CROP_LEFT_MAX	16777215	0xffffffff (in pixels)
CORACQ_CAP_SYNC_CROP_LEFT_MIN	0	0x0 (in pixels)
CORACQ_CAP_SYNC_CROP_LEFT_MULT	1	0x1 (pixel)
CORACQ_CAP_SYNC_CROP_TOP_MAX	16777215	0xffffffff (in lines)
CORACQ_CAP_SYNC_CROP_TOP_MIN	0	0x0 (in lines)
CORACQ_CAP_SYNC_CROP_TOP_MULT	1	0x1 (line)
CORACQ_CAP_SYNC_CROP_WIDTH_MAX	16777215	0xffffffff (in pixels)
CORACQ_CAP_SYNC_CROP_WIDTH_MIN	0	0x0 (in pixels)
CORACQ_CAP_SYNC_CROP_WIDTH_MULT	1	0x1 (pixel)
CORACQ_CAP_TIME_INTEGRATE_DELAY_MAX	65535000	0x3e7fc18 (in $\mu$ s)
CORACQ_CAP_TIME_INTEGRATE_DELAY_MIN	0	0x0 (in $\mu$ s)
CORACQ_CAP_TIME_INTEGRATE_DURATION_MAX	65535000	0x3e7fc18 (in $\mu$ s)
CORACQ_CAP_TIME_INTEGRATE_DURATION_MIN	1	0x1 (in $\mu$ s)
CORACQ_CAP_VSYNC_REF	2	(0x2) End of vertical sync

# Acquisition Related Capabilities

Capability	Value or Limits or Bitfield	Capability Description / Details
CORACQ_CAP_SIGNAL_STATUS	00110111b	(0x01) CORACQ_VAL_SIGNAL_HSYNC_PRESENT (0x02) CORACQ_VAL_SIGNAL_VSYNC_PRESENT (0x04) CORACQ_VAL_SIGNAL_PIXEL_CLK_PRESENT (0x10) CORACQ_VAL_SIGNAL_HSYNC_LOCK (0x20) CORACQ_VAL_SIGNAL_VSYNC_LOCK

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## X64-CL Memory Error with Area Scan Frame Buffer Allocation

The memory error message [ **Error: "CorXferConnect" <Xfer module> - No memory ()** ] may occur when loading a Sopera camera file, or when the application configures a frame buffer for area scan cameras. The problem is that the X64-CL does not have enough onboard memory for two frame buffers.

The X64-CL when used with area scan cameras, allocates two internal frame buffers in onboard memory, each equal in size to the acquisition frame buffer. This allocation is automatic at the driver level. The X64-CL driver allocates two buffers to ensure that the acquired video frame is complete and not corrupted in cases where the transfer to host system memory may be interrupted by other host system processes.

The total size of the two internal frame buffers must be somewhat smaller than the total onboard memory due to memory overhead required for image transfer management. Also note that the X64-CL Dual board equally divides the onboard memory between the two acquisition modules, reducing the available memory for the two buffers by half.

# X64-CL Sopera Servers & Resources

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## Servers and Resources

Servers		Resources			
Name	Description	Type	Name	Index	Description
X64_1	X64-CL Full	Acquisition	Digital CamLink Full Mono #1	0	Digital CamLink Full configuration, monochrome output, Camera #1
X64_1	X64-CL Dual	Acquisition	Digital CamLink Base Mono #1	0	Digital CamLink Base configuration, monochrome output, Camera #1
			Digital CamLink Base Mono #2	1	Digital CamLink Base configuration, monochrome output, Camera #2
			Digital CamLink Base Color RGB #1	2	Digital CamLink Base configuration, color output, Camera #1
			Digital CamLink Base Color RGB #2	3	Digital CamLink Base configuration, color output, Camera #2

---

# Transfer Resource Locations

The following table illustrates all possible source/destination pairs in a transfer.

Source	Transfer passing through	Destination
X64-CL Acquisition	1 to $2^{17}$ internal buffers	1 to $2^{17}$ Host Buffers
X64-CL Acquisition	1 to $2^{17}$ internal buffers & the X64 internal processor	1 to $2^{17}$ Host Buffers

# Technical Specifications

## Specifications

### General System Requirements for the X64-CL Series

Computer system with a 64 bit – 66/33 MHz PCI slot or a 32 bit – 33 MHz PCI slot.

### Operating System Support

Windows NT 4.0 SP6 and Windows 2000 SP1 and Windows XP

### Digital Video Input

Number	Dependent on Model X64-CL Full: 1 Full or 1 Medium or 1 Base X64-CL Dual: 1 or 2 Base
Common Pixel Formats <i>(see details following)</i>	Monochrome cameras - 8, 10, or 12 bits RGB cameras – 24 bits
Base Configuration Pixel Formats	3 x 8-bit, 2 x 10-bit, 2 x 12-bit, 1 x 14-bit, 1 x 16-bit, 24-bit RGB
Medium Configuration Pixel Formats	4 x 8-bit, 2 x 10-bit, 4 x 10-bit, 2 x 12-bit, 4 x 12-bit, 30-bit RGB <i>(future)</i> , 36-bit RGB <i>(future)</i>
Full Configuration Pixel Formats	8 x 8-bit,
Scanning	Progressive Multi-Tap Multi-Channel Four quadrant Tap reversal
Input LUTs	Yes. See section “X64-CL LUT availability” (page 61) for details.
Resolution  <i>note: these are X64-CL maximums, not CameraLink specifications</i>	Horizontal Minimum: 8 Pixels per tap  Horizontal Maximum: 8-bits/pixel x 256K Pixels/line 16-bits/pixel x 128K Pixels/line 32-bits/pixel x 64K Pixels/line 64-bits/pixel x 32K Pixels/line  Vertical Minimum: 1 line

	Vertical Maximum: up to 16,000,000 lines
Pixel Clock Range	up to 85 MHz dependent on model

### Supported Specialty Cameras

Contact Coreco Imaging support (<http://www.imaging.com/support>) for more information on these cameras and other similar non-standard cameras.

See "Firmware: X64-CL 10-Tap Format 1" on page 63 for more information about the X64-CL support for the Vosskuler CMC-1300.

See "Firmware: X64-CL 10-Tap Format 2" on page 64 for more information about the X64-CL support for the Basler A504k.

### X64-CL Physical Dimensions

Approximately 6.9 in. (17.5 cm) wide by 4.2 in. (10.7 cm) high (conforms to half length PCI)

### Power Requirements

+5 Volt	2 amp typical	<i>Note: other internal voltages are derived from +5V</i>
+12 Volt		<i>As per camera connected and supplied by X64-CL PC power interface</i>

### Environment

Ambient Temperature:	10° to 50° C (operation) 0° to 70° C (storage)
Relative Humidity:	5% to 90% non-condensing (operating) 0% to 95% (storage)

### Certifications

Class B, FCC and CE

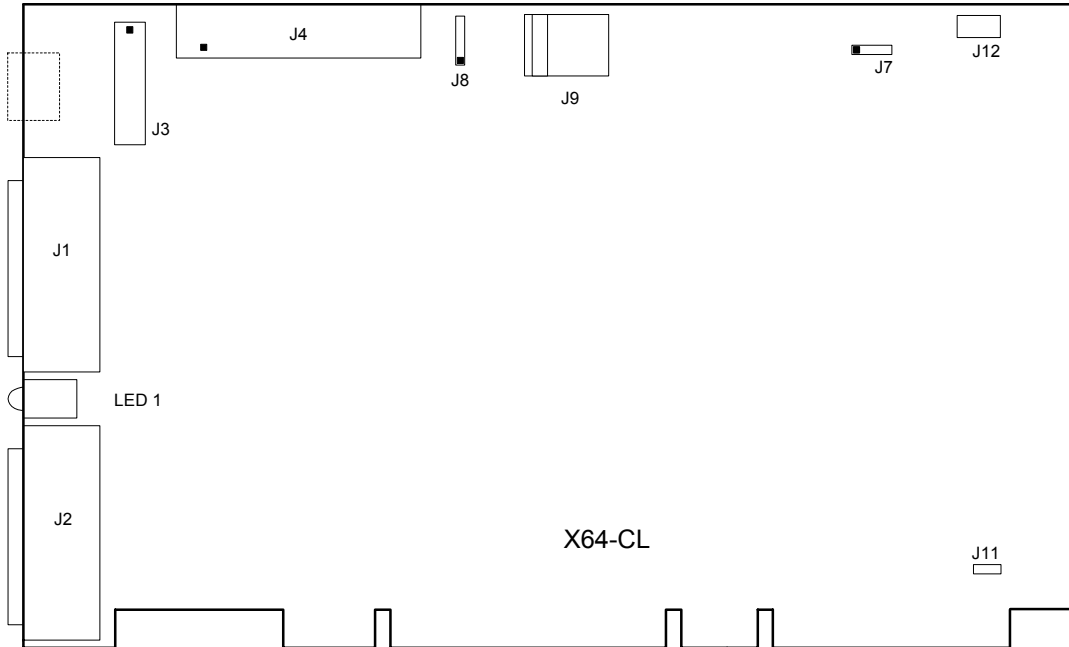
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# Connector and Switch Locations

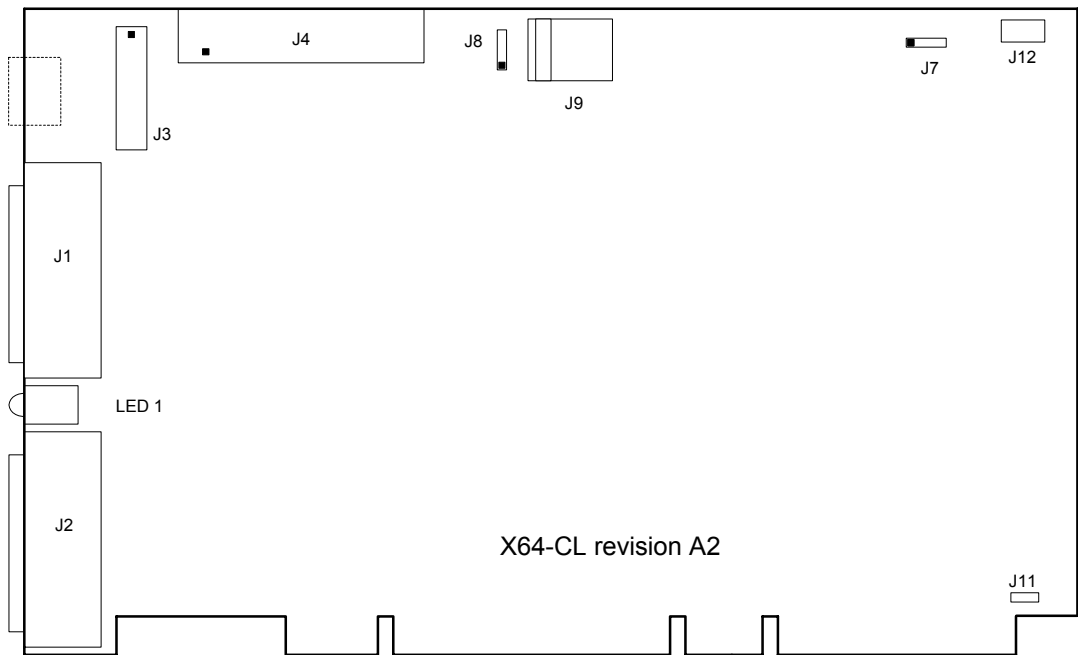
## X64-CL Layout Drawings

The X64-CL with 32MB or 128MB of memory is built on a half length board. As of the printing date of this manual, the X64-CL has been in production in four board revisions (A2, A3, A4, A5). The component view drawings are shown below.

### X64-CL Revision A3, A4, A5 & B0 Layout Drawing



**X64-CL Revision A2 Layout Drawing**

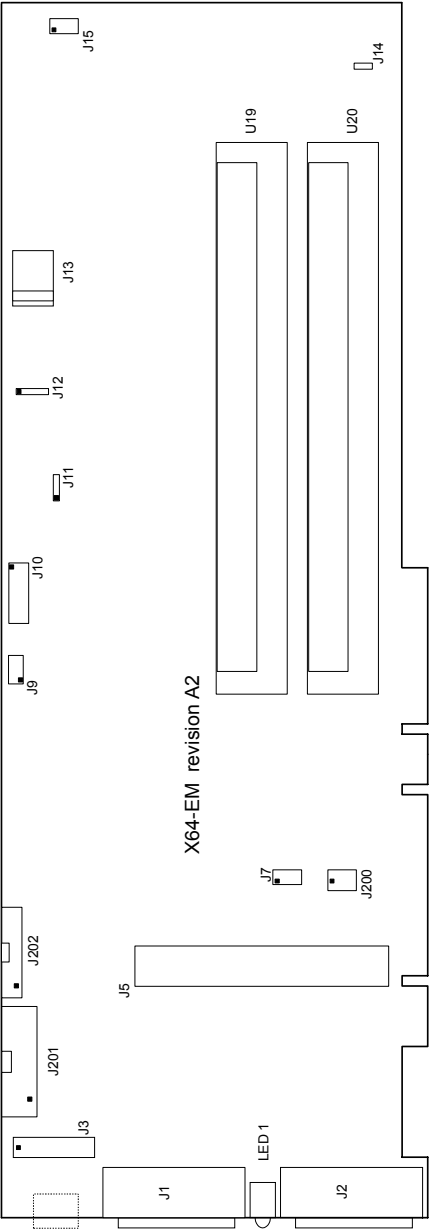


**Connector List (X64-CL half length board)**

Connector	Description	Connector	Description
J1	CamLink Connector	J8	Camera Power Selector
J2	CamLink Connector	J9	PC power to camera interface.
J3	Aux. Module Connector (typical – Hirose)	J11	Normal (jumper on) Safe Start Mode (jumper off)
J4	I/O Connector block	J12	Reserved
J7	Multiple board trigger lock		

# X64-CL EM Revision A2 Layout Drawing

The X64-CL Series boards with 256MB, 1GB, or 2GB of memory, is built on a full length board. For reference purposes, this PCB is called X64-CL EM. The board layout and connector list are shown below.



# Connector List (X64-CL EM full length board)

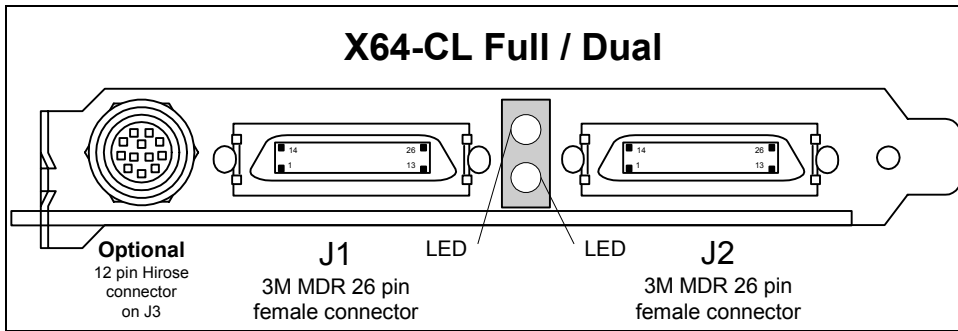
Connector	Description	Connector	Description
J1	CamLink Connector	J11	Multiple board trigger lock
J2	CamLink Connector	J12	Camera Power Selector
J3	Aux. Module Connector (typical – Hirose)	J13	PC power to camera interface.
J5	Connector for CameraLink Expansion module	J14	Normal (jumper on) Safe Start Mode (jumper off)
J201	I/O Connector block	J7, J9, J10, J15, J200	Reserved
J202	Reserved for X64 I/O Module	U19, U20	DDR memory (registered) modules

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# Connector and Switch Specifications

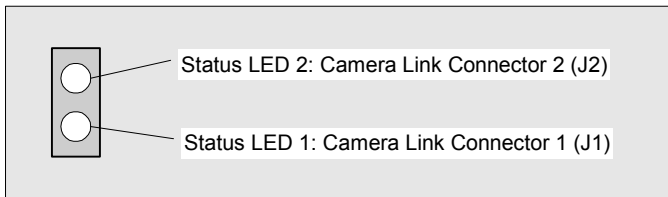
## X64-CL Connector View

The following X64-CL connector bracket view shows the CameraLink connectors, status LEDs and the optional 12 pin Hirose connector module (connected internally to connector J3). Note that some computer cases may not provide the required clearance for the Hirose connector option.



- The **X64-CL Full** board supports a camera with one or two CameraLink MDR-26 connectors (Base or medium or Full – see "Data Port Configuration Table" on page 98 for information on CameraLink configurations).
  - Connect the camera to the X64-CL J1 connector with a CameraLink cable. When using Medium or Full cameras, connect the second camera connector to X64-CL J2.
- The **X64-CL Dual** supports one or two Base CameraLink cameras.
  - Connect the first camera to the X64-CL J1 connector with a CameraLink cable. If using a second camera, connect to X64-CL J2.

## Status LEDs Functional Description



### Status LED Modes

- Red: No camera connected or camera has no power.
- Green: Camera connected and is ON. Camera clock detected. No line valid detected.
- Flashing Green: Camera Line Valid signal detected.
- Status LED 2 flashing red, X64-CL Full board only: Camera pixel clock incorrectly connected to J2 instead of J1. (Example - a Base camera is incorrectly connected to J2).

## J1: CameraLink Connector 1 (applies to X64-CL Dual & Full models)

Name	Pin #	Type	Description
BASE_X0-	25	Input	Neg. Base Data 0
BASE_X0+	12	Input	Pos. Base Data 0
BASE_X1-	24	Input	Neg. Base Data 1
BASE_X1+	11	Input	Pos. Base Data 1
BASE_X2-	23	Input	Neg. Base Data 2
BASE_X2+	10	Input	Pos. Base Data 2
BASE_X3-	21	Input	Neg. Base Data 3
BASE_X3+	8	Input	Pos. Base Data 3
BASE_XCLK-	22	Input	Neg. Base Clock
BASE_XCLK+	9	Input	Pos. Base Clock
SERTC-	20	Output	Neg. Serial Data to Camera
SERTC+	7	Output	Pos. Serial Data to Camera
SERTFG-	19	Input	Neg. Serial Data to Frame Grabber
SERTFG+	6	Input	Pos. Serial Data to Frame Grabber
CC1-	18	Output	Neg. Camera Control 1
CC1+	5	Output	Pos. Camera Control 1
CC2-	17	Output	Neg. Camera Control 2
CC2+	4	Output	Pos. Camera Control 2
CC3-	16	Output	Neg. Camera Control 3
CC3+	3	Output	Pos. Camera Control 3
CC4-	15	Output	Neg. Camera Control 4
CC4+	2	Output	Pos. Camera Control 4
GND	1, 13, 14, 26		Ground

## J2: CameraLink Connector 2 (on X64-CL Dual model)

The CameraLink connector J2 on the X64-CL Dual board is identical to CameraLink connector 1 (J1).

## J2: CameraLink Connector 2 (on X64-CL Full model used with Medium or Full cameras)

Name	Pin #	Type	Description
MEDIUM_X0-	25	Input	Neg. Medium Data 0
MEDIUM_X0+	12	Input	Pos. Medium Data 0
MEDIUM_X1-	24	Input	Neg. Medium Data 1
MEDIUM_X1+	11	Input	Pos. Medium Data 1
MEDIUM_X2-	23	Input	Neg. Medium Data 2
MEDIUM_X2+	10	Input	Pos. Medium Data 2
MEDIUM_X3-	21	Input	Neg. Medium Data 3
MEDIUM_X3+	8	Input	Pos. Medium Data 3
MEDIUM_XCLK-	22	Input	Neg. Medium Clock
MEDIUM_XCLK+	9	Input	Pos. Medium Clock
TERM	20		Term Resistor
TERM	7		Term Resistor
FULL_X0-	19	Input	Neg. Full Data 0
FULL_X0+	6	Input	Pos. Full Data 0
FULL_X1-	18	Input	Neg. Full Data 1
FULL_X1+	5	Input	Pos. Full Data 1
FULL_X2-	17	Input	Neg. Full Data 2
FULL_X2+	4	Input	Pos. Full Data 2
FULL_X3-	15	Input	Neg. Full Data 3
FULL_X3+	2	Input	Pos. Full Data 3
FULL_XCLK-	16	Input	Neg. Full Clock
FULL_XCLK+	3	Input	Pos. Full Clock
GND	1, 13, 14, 26		Ground

## CameraLink Camera Control Signal Overview

Four LVDS pairs are for general-purpose camera control, defined as camera inputs / frame grabber outputs by the CameraLink Base camera specification. These controls are on J1 (X64-CL Full and X64-CL Dual) and also on J2 for the second Base camera input of the X64-CL Dual.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

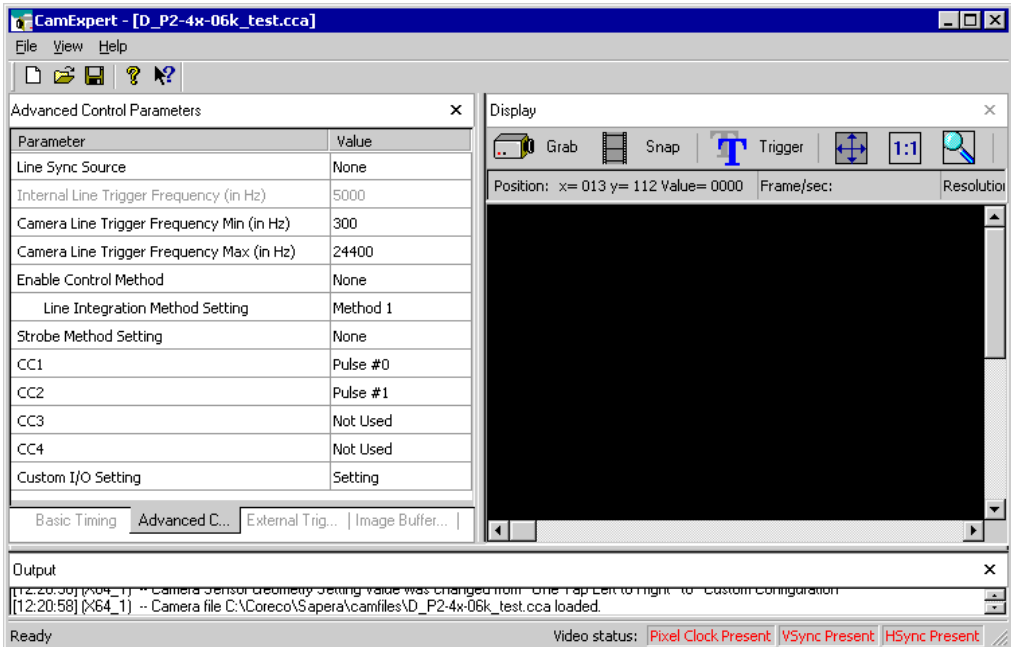
Each camera manufacture is free to define the signals input on any one or all four control signals. These control signals are used either as camera control pulses or as a static logic state. Control signals not required by the camera are simply assigned as not used. Refer to your camera's user manual for information on what control signals are required.

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Note: The X64-CL pulse controller has a minimum resolution of 1 us. When configuring the CameraLink control signals, such as exposure control, etc. use values in increments of 1 us.

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The X64-CL can assign any camera control signal to the appropriate CameraLink control. The following screen shot shows the Spera CamExpert dialog where CameraLink controls are assigned.



## J4 (CL) (EM rev. A0, A1): I/O Connector Block

### J4 Pin Header Numbering Detail

2	4	...	24	26
1	3	...	23	25

### J4 Signal Descriptions

Pin #	Signal	X64-CL Full Description	X64-CL Dual Description
1		Reserved	Reserved
2, 4, 6	GND		
3		Reserved	Reserved
5		Reserved	Reserved
7		Reserved	Reserved
8		Reserved	Reserved
9		Reserved	Reserved
10		Reserved	Reserved
11	TrigIn 1 + (input)	LVDS Trigger In + or TTL Trigger In (see note 1)	CamLink Base #1 LVDS + or TTL Trigger In (see note 2)
12	TrigIn 1 - (input)	LVDS Trigger In - (or TTL Trigger In GND)	CamLink Base #1 LVDS Trigger - (or TTL Trigger GND)
13	TrigIn 2 + (input)	LVDS Trigger In + or TTL Trigger In (Used for two pulse external trigger with variable frame length linescan acquisition)	CamLink Base #2 LVDS + or TTL Trigger In (see note 2)
14	TrigIn 2 - (input)	LVDS Trigger In - (or TTL Trigger In GND)	CamLink Base #2 LVDS Trigger - (or TTL Trigger GND)
15	Phase A + (input)	LVDS/RS422 Shaft Encoder phase A + used with linescan cameras (see note 3 & 4 & 9)	LVDS/RS422 Shaft Encoder + used with linescan cameras (see note 5 & 9)
16	Phase A - (input)	LVDS/RS422 Shaft Encoder phase A - (see note 9)	LVDS/RS422 Shaft Encoder - (see note 9)
17	Phase B + (input)	LVDS/RS422 Shaft Encoder phase B + used with linescan cameras (see note 3 & 4 & 9)	LVDS/RS422 Shaft Encoder + used with linescan cameras (see note 5 & 9)
18	Phase B - (input)	LVDS/RS422 Shaft Encoder phase B - (see note 9)	LVDS/RS422 Shaft Encoder - (see note 9)

19	Strobe 2 (output)	<i>not used</i>	CamLink Base #2 TTL Strobe Output (see note 7)
20		Reserved	
21	Strobe 1 (output)	TTL Strobe Output (see note 6)	CamLink Base #1 TTL Strobe Output (see note 7)
22, 24, 26	GND		
23, 25	DC Power (see note 8)	Voltage selected (+12 or +5) via J8 (see "J8 (CL), J12 (CL EM): Power to Camera Voltage Selector" on page 93)	Voltage selected (+12 or +5) via J8 (see "J8 (CL), J12 (CL EM): Power to Camera Voltage Selector" on page 93)

## Notes for X64-CL Full or X64-CL Dual I/O Connector

### 1. X64-CL Full:

Refer to Spera parameters CORACQ\_PRM\_EXT\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_FRAME\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_TRIGGER\_ENABLE  
CORACQ\_PRM\_EXT\_TRIGGER\_DETECTION

See also \*.cvi file entries:

External Trigger Level, External Frame Trigger Level, External Trigger Enable, External Trigger Detection.

### 2. X64-CL Dual:

Spera parameter CORACQ\_PRM\_EXT\_TRIGGER\_LEVEL,  
CORACQ\_PRM\_EXT\_FRAME\_TRIGGER\_LEVEL is a common control to both CamLink  
Base #1 and #2.

Parameters CORACQ\_PRM\_EXT\_TRIGGER\_ENABLE and  
CORACQ\_PRM\_EXT\_TRIGGER\_DETECTION are independent for each CameraLink input.

See also \*.cvi file entries:

External Trigger Level, External Frame Trigger Level, External Trigger Enable, External Trigger Detection.

### 3. X64-CL Full:

See "Line Trigger Source Selection for Linescan Applications" on page 48 for more information.

Refer to Spera parameters CORACQ\_PRM\_SHAFT\_ENCODER\_ENABLE  
CORACQ\_PRM\_SHAFT\_ENCODER\_DROP

or refer to CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_ENABLE

CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_DETECTION

CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_LEVEL (fixed at LVDS)

CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE

See also \*.cvi file entries:

Shaft Encoder Enable, Shaft Encoder Pulse Drop

or see External Line Trigger Enable, External Line Trigger Detection, External Line Trigger Level, External Line Trigger Source.

### 4. X64-CL Full:

Important: When using only one shaft encoder input phase, say phase A, then the phase B inputs

must be terminated by connecting phase B- to board ground available on any pin labeled GND and phase B+ to any DC source with a minimum of 100 mV positive relative to the phase B- input.

5. **X64-CL Dual:**

Same parameters as X64-CL Full (see note 3).

Parameters are independent for CamLink Base #1 and #2.

6. **X64-CL Full:**

Refer to Sapera parameters CORACQ\_PRM\_STROBE\_ENABLE  
CORACQ\_PRM\_STROBE\_POLARITY, CORACQ\_PRM\_STROBE\_LEVEL,  
CORACQ\_PRM\_STROBE\_METHOD, CORACQ\_PRM\_STROBE\_DELAY  
CORACQ\_PRM\_STROBE\_DURATION

See also \*.cvi file entries:

Strobe Enable, Strobe Polarity, Strobe Level, Strobe Method, Strobe Delay, Strobe Duration.

7. **X64-CL Dual:**

Same parameters as X64-CL Full (see note 6).

Parameters are independent for CamLink Base #1 and #2.

8. **DC Power Constraints:**

The supplied host PC voltage is selected (+12 or +5) via the shorting jumper J8 (see "J8 (CL), J12 (CL EM): Power to Camera Voltage Selector" on page 93 for details).

*Important.*

For **X64-CL revision A2, A3, A4** boards, the selected voltage is *not* fused. It is strongly recommended that any cabling using the DC power has an inline fuse (1.5A max).

For **X64-CL revision A5 and later** boards, a 1.5A resettable fuse is included on the board. If the fuse is tripped, power off the host computer to reset the fuse.

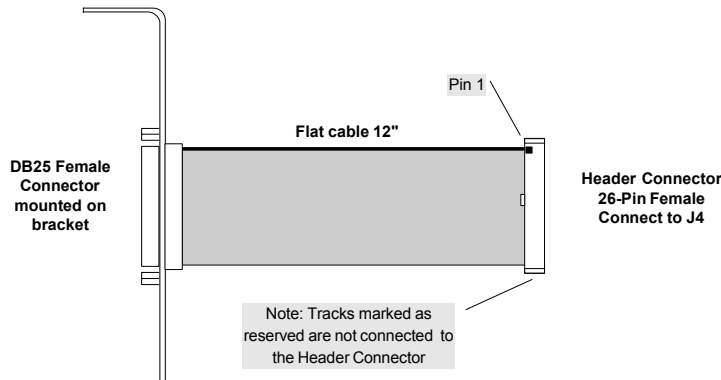
9. See "Connecting a TTL Shaft Encoder Signal to the LVDS/RS422 Input" on page 92 for details on using a TTL shaft encoder signal.

# X64-CL I/O Connector Bracket Assembly

The I/O Connector Bracket Assembly (part number OC-64CC-0TIO1) applies to the short length X64-CL board with 32 or 128 MB of memory. For the X64-CL EM full length board with 256MB, 1GB, or 2GB see .

The I/O connector bracket provides a simple way to bring out the signals from the X64-CL I/O connector J4 to a bracket mounted DB25. Install the bracket assembly into an adjacent PC expansion slot and connect the free cable end to the X64-CL J4 header. When connecting to J4, make sure that the cable pin 1 goes to J4 pin 1 (see layout drawings for your board revision: "X64-CL Layout Drawings" on page 77).

## I/O Connector Bracket Assembly Drawing



## I/O Connector Bracket Assembly Signal Description

Refer to the table "J4 (CL) (EM rev. A0, A1): I/O Connector Block" on page 86 for important signal descriptions.

DB25 Pin Number	Signal Names	Connector (to J4)
1, 2, 3, 4, 17, 5, 18, 23, 12, 13	Reserved	1, 3, 5, 7, 8, 9, 10, 20, 23, 25
6	TrigIn 1+	11
19	TrigIn 1-	12
7	TrigIn 2+	13
20	TrigIn 2-	14
8	Shaft Encoder phase A +	15
21	Shaft Encoder phase A -	16
9	Shaft Encoder phase B +	17
22	Shaft Encoder phase B -	18
11	Strobe 1	21
10	Strobe 2	19
14, 15, 16, 24, 25,	Ground	2, 4, 6, 22, 24

## J201 (EM rev. A2 & later): I/O Connector Block

Contact Coreco Imaging for information on the I/O Connector Bracket Assembly to bring out the signals from the X64-CL EM I/O connector J201 to a bracket mounted connector.

Pin #	Signal	X64-CL EM Description
1	Trig1+	External Trigger 1 + input <i>see note 1</i>
2	Trig1-	External Trigger 1 - input
3	Trig2+	External Trigger 2 + input
4	Trig2-	External Trigger 2 - input
5	PHA+	Shaft Encoder Phase A + <i>see note 2 &amp; 3 &amp; 4</i>
6	PHA-	Shaft Encoder Phase A -
7	PHB+	Shaft Encoder Phase B +
8	PHB-	Shaft Encoder Phase B -
9	STROBE2	Strobe control 2 (TTL)
10	Reserved	Reserved
11	STROBE1	Strobe control 1 (TTL) <i>see note 5</i>
12		Reserved
13		Reserved
14	GND	Ground
15	DC Power	Voltage selected (+12 or +5) via J8 <i>see note 6</i>
16		Reserved

### Notes for X64-CL EM I/O Connector

1. Refer to Spera parameters  
CORACQ\_PRM\_EXT\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_FRAME\_TRIGGER\_LEVEL  
CORACQ\_PRM\_EXT\_TRIGGER\_ENABLE  
CORACQ\_PRM\_EXT\_TRIGGER\_DETECTION
2. See "Line Trigger Source Selection for Linescan Applications" **on page 48** for more information.  
Refer to Spera parameters CORACQ\_PRM\_SHAFT\_ENCODER\_ENABLE  
CORACQ\_PRM\_SHAFT\_ENCODER\_DROP  
or refer to CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_ENABLE  
CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_DETECTION  
CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_LEVEL (fixed at LVDS)  
CORACQ\_PRM\_EXT\_LINE\_TRIGGER\_SOURCE

3. Important: When using only one shaft encoder input phase, say phase A, then the phase B inputs must be terminated by connecting phase B- to board ground available on any pin labeled GND and phase B+ to any DC source with a minimum of 100 mV positive relative to the phase B-input.
4. See "Connecting a TTL Shaft Encoder Signal to the LVDS/RS422 Input" on page 92 for details on using a TTL shaft encoder signal.
5. Refer to Sopera parameters CORACQ\_PRM\_STROBE\_ENABLE  
CORACQ\_PRM\_STROBE\_POLARITY, CORACQ\_PRM\_STROBE\_LEVEL,  
CORACQ\_PRM\_STROBE\_METHOD, CORACQ\_PRM\_STROBE\_DELAY  
CORACQ\_PRM\_STROBE\_DURATION
6. The supplied host PC voltage is selected (+12 or +5) via the shorting jumper J8. A 1.5A resettable fuse is included on the board. If the fuse is tripped, power off the host computer to reset the fuse.

## Hirose Connector Module Option (connects internally to J3)

The 12 pin Hirose connector option is available by special order. Contact sales at Coreco Imaging for information about this factory installed option.

Pin #	Signal	Description
1	Power	5V or 12V selectable with Jumper J8 for Camera Power (1.5A max)
2	GND	Ground for Camera
8	TrigIn 1+	TTL Trigger 1 In or LVDS Trigger 1 In +  <i>TTL or LVDS is selected by the Sopera VIC parameter External Trigger Level or External Frame Trigger Level or the Sopera parameter CORACQ_PRM_EXT_TRIGGER_LEVEL or CORACQ_PRM_EXT_FRAME_TRIGGER_LEVEL</i>
7	TrigIn 1-	LVDS Trigger 1 In - (or TTL Trigger 1 In GND)
9	TrigIn 2+	TTL Trigger 2 In or LVDS Trigger 2 In +
6	TrigIn 2-	LVDS Trigger 2 In - (or TTL Trigger 2 In GND)
12	Phase A +	LVDS Shaft Encoder phase A + (or phase A TTL input +)
5	Phase A -	LVDS Shaft Encoder phase A - (see "Connecting a TTL Shaft Encoder Signal to the LVDS/RS422 Input" on page 92 for details on using a TTL shaft encoder signal).
10	Phase B +	LVDS Shaft Encoder phase B + (or phase B TTL input +)
4	Phase B -	LVDS Shaft Encoder phase B - (see "Connecting a TTL Shaft Encoder Signal to the LVDS/RS422 Input" on page 92 for details on using a TTL shaft encoder signal).
11	Strobe 1	TTL Strobe 1 output : to connect to a strobe lamp
3	Strobe 2	TTL Strobe 2 output : to connect to a strobe lamp

---

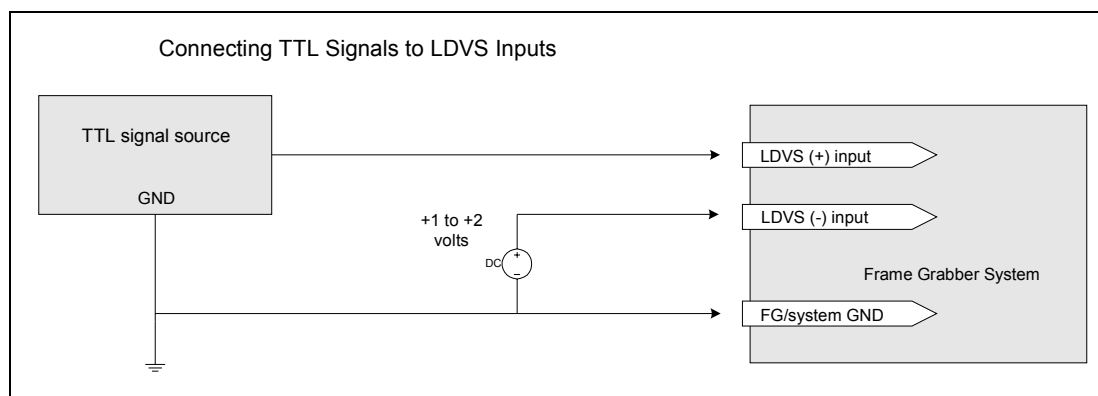
Important: When using only one shaft encoder input phase with a X64-CL Full, say phase A, then the phase B inputs must be both terminated by connecting phase B- to board ground available on any pin labeled GND and phase B+ to any DC source with a minimum of +100 mV relative to ground.

---

## Connecting a TTL Shaft Encoder Signal to the LVDS/RS422 Input

A TTL shaft encoder signal can be directly connected to the X64-CL LVDS/RS422 (+) input but the low side (-) input of the pair must be biased with a DC voltage to ensure reliable operation. This section shows the connection diagram along with suggestions as to how to generate the DC bias voltage. The actual physical wiring is left as an additional detail to interfacing a shaft encoder to the X64-CL to the imaging system.

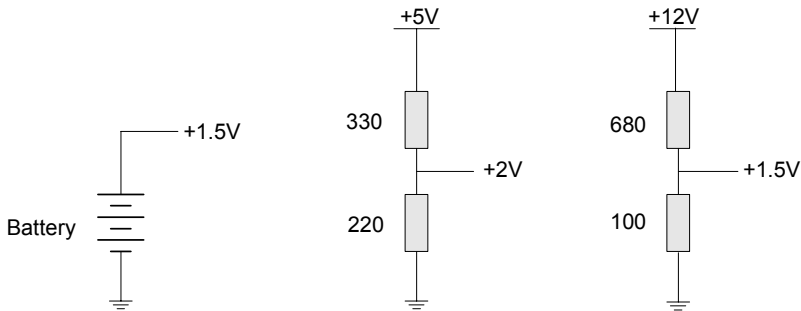
### TTL Shaft Encoder to LVDS/RS422 Input Block Diagram



- LVDS/RS422 (-) input is biased to a DC voltage from +1 to +2 volts.
- This guarantees that the TTL signal connected to the LVDS/RS422 (+) input will be detected as a logic high or low relative to the (-) input.
- The TTL shaft encoder ground, the bias voltage ground, and the X64-CL computer system ground must be connected together.

## LVDS/RS422 (-) Input Bias Source Generation

### 3 Examples on Generating a DC voltage for the LDVS (-) Input



- DC voltage for the LVDS/RS422 (-) input can be generated by a resistor voltage divider.
- Use a single battery cell if this is more suitable to your system.
- A DC voltage (either +5 or +12) is available on I/O connector J4. See "J8 (CL), J12 (CL EM): Power to Camera Voltage Selector" on page 93 for information.

## J8 (CL), J12 (CL EM): Power to Camera Voltage Selector

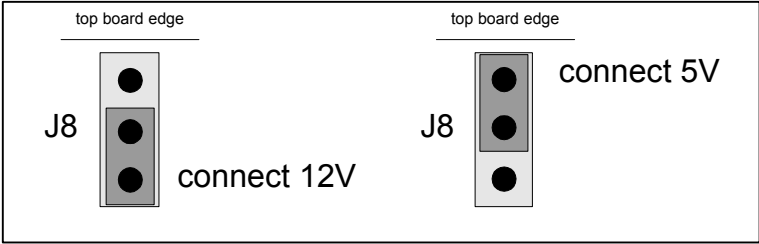
When the PC floppy drive power supply cable is connected to J9/J13, a shorting jumper on J8/J12 selects either 5 Vdc or 12 Vdc for the camera power supply. This supply voltage is available on the Hirose connector module or on the I/O connector block.

### Important:

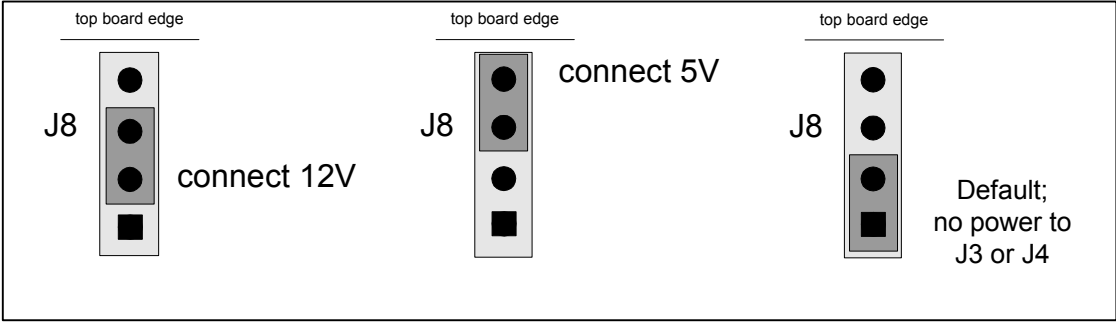
For **X64-CL revision A2, A3, A4** boards, the selected voltage is *not* fused. It is strongly recommended that any cabling using the DC power has an inline fuse (1.5A max).

For **X64-CL revision A5 and later** boards, or **X64-CL EM A2** boards, a 1.5A resettable fuse is included on the board. If the fuse is tripped, power off the host computer to reset the fuse.

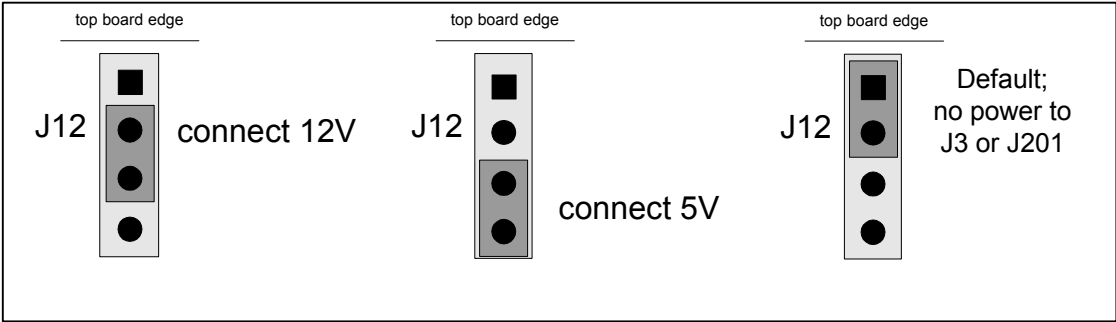
**J8 as on X64-CL revision A1 and A2 boards**



**J8 as on X64-CL revision A3, A4, A5 boards**



**J12 as on X64-CL EM revision A2 board**



## **J9 (CL), J13 (CL EM): PC Power to Camera Interface**

Connect the PC floppy drive power connector to J9/J13 so as to supply DC power to the camera. Place the J8/J12 shorting jumper so as to select 5 Vdc or 12 Vdc for the camera.

## **J11 (CL), J14 (CL EM): Start Mode**

- Default Mode: Shunt jumper is installed.
- Safe Mode: Shunt jumper is removed if any problems occurred while updating the X64 firmware. With the jumper off, reboot the computer and update the firmware again. When the update is complete, install the jumper and reboot the computer once again.

## **J7, J12 (CL): Reserved**

## **J7, J9, J10, J11, J15, J200, J202 (CL EM): Reserved**

## Brief Description of Standards RS-232, RS-422, & RS-644 (LVDS)

### RS-232

Short for *recommended standard-232C*, a standard interface approved by the Electronic Industries Association (EIA) connecting serial devices.

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The standards for RS-232 and similar interfaces usually restrict RS-232 to 256kbps or less and line lengths of 15M (50 ft) or less.

---

**Transmitted Data (TxD)** This signal is active when data is transmitted from the DTE device to the DCE device. When no data is transmitted, the signal is held in the mark condition (logic '1', negative voltage).

**Received Data (RxD)** This signal is active when the DTE device receives data from the DCE device. When no data is transmitted, the signal is held in the mark condition (logic '1', negative voltage).

DTE (Data Terminal Equipment)

DCE (Data Communication Equipment)

### RS-422

RS-422 uses a twisted-pair wire (i.e., 2 wires) for each signal. The differential drive voltage swing is 0 to +5V. RS-422 does not have tri-state capability (its driver is always enabled) and it is therefore usable only in point-to-point communications.

Although RS-422 is noise resistant, due to being differential data can still be damaged by EMI/RFI. A shielded cable can protect the transmitters/receivers from EMI/RFI.

### RS-664 (LVDS)

LVDS (Low-Voltage Differential Signaling): method to communicate data using a very low voltage swing (about 350mV) over two differential PCB traces or a balanced cable. LVDS allows single channel data transmission at hundreds of Megabits per second (Mbps).

# CameraLink Interface

---

## CameraLink Overview

CameraLink is a communication interface for vision applications developed as an extension of National Semiconductor's Channel Link technology. The advantages of the CameraLink interface are that it provides a standard digital camera connection specification, a standard data communication protocol, and simpler cabling between camera and frame grabber.

The CameraLink interface simplifies the usage of increasingly diverse cameras and high signal speeds without complex custom cabling. For additional information concerning CameraLink, see <http://www.pulnix.com/>.



## Rights and Trademarks

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Note: The following text is extracted from the CameraLink Specification (October 2000).

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PULNiX America, Inc., as chair of this ad hoc CameraLink committee, has applied for U.S. trademark protection for the term "CameraLink" to secure it for the mutual benefit of industry members. PULNiX will issue a perpetual royalty-free license to any industry member (including competitors) for the use of the "CameraLink" trademark on the condition that it is used only in conjunction with products that are fully compliant to this standard. PULNiX will not require licensed users of the trademark to credit PULNiX with ownership.

3M™ is a trademark of the 3M Company.

Channel Link™ is a trademark of National Semiconductor.

Flatlink™ is a trademark of Texas Instruments.

Panel Link™ is a trademark of Silicon Image.

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## Data Port Summary

The CameraLink interface has three configurations. A single CameraLink connection is limited to 28 bits requiring some cameras to have multiple connections or channels. The naming conventions for the three configurations are:

- Base: Single Channel Link interface, single cable connector.
- Medium: Two Channel Link interface, two cable connectors.
- Full: Three Channel Link interface, two cable connectors.

## Data Port Configuration Table

A single CameraLink port is defined as having an 8-bit data word. The "Full" specification supports 8 ports labeled as A to H.

Configuration	Ports Supported	X64-CL Connector Used
Base	A, B, C	J1
Medium	A, B, C, D, E, F	J1 & J2
Full	A, B, C, D, E, F, G, H	J1 & J2

---

## Camera Signal Summary

### Video Data

Four enable signals are defined as:

- FVAL Frame Valid (FVAL) is defined HIGH for valid lines.
- LVAL Line Valid (LVAL) is defined HIGH for valid pixels.
- DVAL Data Valid (DVAL) is defined HIGH when data is valid.
- Spare A spare has been defined for future use.

All four enables must be provided by the camera on each Channel Link. All unused data bits must be tied to a known value by the camera.

### Camera Controls

Four LVDS pairs are reserved for general-purpose camera control, defined as camera inputs and frame grabber outputs.

- Camera Control 1 (CC1)
- Camera Control 2 (CC2)
- Camera Control 3 (CC3)
- Camera Control 4 (CC4)

## Communication

Two LVDS pairs have been allocated for asynchronous serial communication to and from the camera and frame grabber. Cameras and frame grabbers should support at least 9600 baud.

- SerTFG Differential pair with serial communications to the frame grabber.
- SerTC Differential pair with serial communications to the camera.

The serial interface protocol is one start bit, one stop bit, no parity, and no handshaking.

---

## CameraLink Cables

For additional information on CameraLink cables and their specifications, visit the following web sites:

3 M	<a href="http://www.3m.com/">http://www.3m.com/</a> (enter <i>CameraLink</i> as the search keyword)
Nortech Systems	<a href="http://www.nortechsys.com/">http://www.nortechsys.com/</a>



# Coreco Imaging Contact Information

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## Sales Information

Visit our web site:

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# Technical Support

**Any support question or request can be submitted via our web site:**

Technical support form via our web page: Support requests for imaging product installations, Support requests for imaging applications	<a href="http://www.imaging.com/support">http://www.imaging.com/support</a>
Camera support information	<a href="http://www.imaging.com/camsearch">http://www.imaging.com/camsearch</a>
Product literature and driver updates	<a href="http://www.imaging.com/download">http://www.imaging.com/download</a>

# Glossary of Terms

## **Bandwidth**

Describes the measure of data transfer capacity. PCI devices must share the maximum PCI bus bandwidth when transferring data to and from system memory or other devices.

## **CAM**

Sapera camera file that uses the file extension CCA by default. Files using the CCA extension, also called CAM files (CORECO CAMERA files), contain all parameters which describe the camera video signal characteristics and operation modes (i.e. what the camera outputs).

## **Channel**

Camera data path that includes all parts of a video line.

## **Checksum**

A value used to ensure data is stored without error. It is created by calculating the binary values in a block of data using some algorithm and storing the results with the data.

## **CMI**

**C**lient **M**odification **I**nstruction. A client requested engineering change applied to a Coreco Imaging board product to support either a non-standard function or custom camera.

## **Contiguous memory**

A block of physical memory, occupying consecutive addresses.

## **CRC**

Proprietary Sapera raw image data file format that supports any Sapera buffer type and utilizes an informative file header. Refer to the *Sapera Basic Modules Reference Manual* “Buffer File Formats” section.

## **Firmware**

Software such as a board driver that is stored in nonvolatile memory mounted on that board.

## **Frame buffer**

An area of memory used to hold a frame of image data. A frame buffer may exist on the acquisition hardware or be allocated by the acquisition hardware device driver in host system memory.

**Grab**

Acquiring an image frame by means of a frame grabber.

**Host**

Refers to the computer system that supports the installed frame grabber.

**Host buffer**

Refers to a frame buffer allocated in the physical memory of the host computer system.

**LSB**

Least Significant Bit in a binary data word.

**MSB**

Most Significant Bit in a binary data word.

**PCI 32**

Peripheral Component Interconnect. The PCI local bus is a 32-bit high-performance expansion bus intended for interconnecting add-in boards, controllers, and processor/memory systems.

**PCI 64**

A superset of the PCI specification providing a 64 bit data path and a 66 MHz clock.

**Pixel**

Picture Element. The number of pixels describes the number of digital samples taken of the analog video signal. The number of pixels per video line by the number of active video lines describes the acquisition image resolution. The binary size of each pixel (i.e., 8-bits, 15-bits, 24-bits) defines the number of gray levels or colors possible for each pixel.

**RAW**

A Sapera data file format where there is no header information and that supports any Sapera buffer type. Refer to the *Sapera Basic Modules Reference Manual* “Buffer File Formats” section.

**RISC**

(Reduced Instruction Set Computer) A computer architecture that reduces chip complexity by using simpler instructions.

**Scatter Gather**

Host system memory allocated for frame buffers that is virtually contiguous but physically scattered throughout all available memory.

**Tap**

Data path from a camera that includes a part of or whole video line. When a camera tap outputs a partial video line, the multiple camera tap data must be constructed by combining the data in the correct order.

**VIC**

Sapera camera parameter definition file that uses the file extension CVI by default. Files using the CVI extension, also known as VIC files (CORECO VIDEO files), contain all operating parameters related to the frame grabber board (i.e. what the frame grabber can actually do with camera controls or incoming video).



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